Resurrecting Dated ATE for High Speed Serdes Testing
Mohamed Hafed, PhD & Paul Sakamoto
DFT Microsystems Inc.
www.dftmicrosystems.com
Problem Statement

• SerDes is making its way to all device classes
  – Technological reasons: chips run faster, cooler
  – Market reasons: HD Video everywhere

• SerDes testing is difficulties:
  – Complex “digital” protocols
  – Subtle “analog” measurements
  – Measuring noise and noise tolerance
Problem Statement

- Traditional ATE approach to SerDes test is too expensive for Consumer device market
  - Expensive instruments for high-end server and communications markets
- Installed Base ATE has insufficient capability
  - Legacy ATE: No OEM support vs. new system sales
  - In-house ATE: Big development to add capability
  - OSAT: Same issues as In-House ATE
Proposed Solution

Legacy ATE + Focused SerDes Port Tester = Optimized Test Solution

- Benefit from the cost of legacy ATE
- Benefit from the flexibility of modern SerDes Port Tester
 Agenda

• The need to “connect” to SerDes
  – Plug-and-play testing
• Focused SerDes port tester description
• Experimental Results and Correlation with Bench Equipment
• Case Study: 800 Mbps MIPI wafer-level test on 40 MHz ATE
• Conclusion
The Need to “Connect”

Modern interfaces need a complex hand-shake before they can be tested!

Typical Modern Signal (MIPI)
The Need to “Connect”

- Test access ports are disappearing due to high integration levels
- Testing the transistors inside the “core” of the device has to occur through the protocol
6.4 Gbps SerDes Port Tester

Natively capable of PHY tests due to integration of AC parametric circuitry

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Jitter Analyzer
Pattern Generator
BERT
Oscilloscope
Jitter Injector

8 Lanes
Flexible Architecture

- Maintain the usual digital pattern handling capability that we expect from a digital ATE
• For each time-base generator delay setting, the change in delay due to a 10°C rise in temperature is displayed.
Key Technologies

Clock Recovery

• Single DUT response measured with and without clock recovery

• Low frequency jitter is completely tracked with internal Clock Recovery

No Clock Recovery

Internal Clock Recovery
Key Technologies

Waveform-Based Jitter Injection

- Like time-base generator, jitter injection logic is high purity and compact

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Experimental Results

- A single DUT was measured using the SerDes port focused tester and using an Agilent Infiniium DSO81304B 13 GHz oscilloscope.
- The objective was to evaluate signal fidelity on the ATE.
3.2 Gbps Eye Comparison
3.2 Gbps Eye Comparison

Overlay
PCle Comparison

Agilent DSO capture

SerDes Port Tester capture
PCle Comparison

Overlay

Eye Diagram - Channel 3

phase delay (ps)

voltage (mV)

BER Diagram

BER Contour

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Silicon Valley Test Conference 2010
Case Study: MIPI DSI

Objective: Memory Test of Display Device

- Fully-autonomous handshake through the DSI protocol (D-PHY)
- I/O test is only secondary to full memory test
- Need a protocol exerciser on ATE!
Customized Test Processor

- Main pattern memory
- Additional LP and sequencer blocks
- Additional LP Rx compare

Diagram showing:
- PLLs
- Pattern memory
- Pattern memory arbiter
- HS Pattern generator
- LP Pattern generator
- Sequencer
- Rx Comp
- LP Rx
Entire flow chart is implemented inside FPGA operating system.
### Programming Model

**Step 1: Develop program on bench (high-level commands in CSV format)**

<table>
<thead>
<tr>
<th>State</th>
<th>MIPI Data Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTRL</td>
<td>EME</td>
<td>1 DI=29 (Generic Write, Long)</td>
</tr>
<tr>
<td>CTRL</td>
<td>LPDT</td>
<td></td>
</tr>
<tr>
<td>LP-TX</td>
<td>29</td>
<td>2 WC(0)=05</td>
</tr>
<tr>
<td>LP-TX</td>
<td>5</td>
<td>3 WC(1)=00, WordCount = 0005 = 5 bytes</td>
</tr>
<tr>
<td>LP-TX</td>
<td>0</td>
<td>4 ECC</td>
</tr>
<tr>
<td>LP-TX</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>LP-TX</td>
<td>D0</td>
<td>1 MCSON (D0h)</td>
</tr>
<tr>
<td>LP-TX</td>
<td>1</td>
<td>2 parameter 1 = 01 = MCS function ON</td>
</tr>
<tr>
<td>LP-TX</td>
<td>5A</td>
<td>3 parameter 2 = 5A = hardcoded, part of command</td>
</tr>
<tr>
<td>LP-TX</td>
<td>A5</td>
<td>4 parameter 3 = A5 = hardcoded, part of command</td>
</tr>
<tr>
<td>LP-TX</td>
<td>6C</td>
<td>5 parameter 4 = 6C = hardcoded, part of command</td>
</tr>
<tr>
<td>LP-TX</td>
<td>B0</td>
<td>0 checksum (CRC)</td>
</tr>
<tr>
<td>LP-TX</td>
<td>5B</td>
<td>0 checksum (CRC)</td>
</tr>
<tr>
<td>CTRL</td>
<td>Mark-1</td>
<td></td>
</tr>
<tr>
<td>CTRL</td>
<td>EME</td>
<td>1 DI=13 (Generic Write, 1 parameter)</td>
</tr>
<tr>
<td>CTRL</td>
<td>LPDT</td>
<td></td>
</tr>
<tr>
<td>LP-TX</td>
<td>13</td>
<td>2 Data(0)=B5 (DISSET3, AREFOFF=1)</td>
</tr>
<tr>
<td>LP-TX</td>
<td>B5</td>
<td></td>
</tr>
</tbody>
</table>

**Step 2: Compile csv program and store on test module**

- Simple interpretation is performed inside the FPGA for executing the test
Conclusion

• We have presented a mechanism by which low-speed ATE can test high-speed digital interfaces
• The solution is based on a SerDes test module that offers low cost and high flexibility
• We have provided experimental results and case studies to demonstrate (a) the need for a new way to test high-speed digital interfaces and (b) a proven solution for doing so