IJTAG Test Strategy for 3D IC Integration
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Why 3D?

So, who suffers? Fab Tool Providers… they only have 5 customers left…

Fabs: not as popular as they used to be

| Altis Semiconductor | Dongbu Hitek | Freescale | Fujitsu | Globalfoundries | Grace Semiconductor | IBM | Intel | Panasonic | Renesas (NEC) | Samsung | Seiko Epson | SMIC | Sony | ST Microelectronics | Texas Instruments | Toshiba | TSMC | UMC | 130nm | 90nm | 65nm/55nm | 45/40nm | 32/28nm | 22/20nm |
|---------------------|-------------|-----------|---------|-----------------|---------------------|-----|-------|-----------|--------------|---------|-------------|------|------|---------------------|------------------|--------|------|-----|--------|--------|----------|----------|---------|--------|---------|
|                     |             |           |         |                 |                     |     |       |           |              |         |             |      |      |                      |                  |         |      |     |        |        |          |          |         |        |        |

As process size shrinks, so do the number of fabs able to produce chips at those geometries (click to enlarge)
3D Packaging vs 3D ICs

3-D Packaging to 3-D IC Integration

- Through-silicon (wafer) vias (TSVs)
- Wafer thinning
- Wafer (die) bonding
3D TSV’s

- Via Size + Keep-Out Zone
- Via Pitch / Bump Pitch
- Logic Spreading to accommodate TSVs
  - e.g. 300K TSV’s consume 1mm²

Direct probing may result in potential damage
Note: no ESD protection

Top of Die

Strap Connection to Internal Route from TSV

Bottom of Die

No logic/routes in this area
Keep-Out Zone

Internal Routes from Layout

Drill & Fill Via

Power & Ground Signal from Brd Signal from Die

Bump Pitch

Bump Size

Via Size

Via Pitch
The 3D Stack

- FPGA Die
- Interposer
- Upper Die
- Upper Die
- Interposer
- Base Die
3D Now vs 3D Future

- Flat Layout & N-S/E-W space
- Routing N-S/E-W lengths
- Stacking TSV displacement
- Today’s CAD/CAE Tools

- Vertical Layout from the start
- Core/Elevators at heart of design
- Routing distance is X, Y, or Z
- Stack Engineering New CAD/CAE
The 3D Die Concerns

- Embedded Test-Debug Access
- Probe Pads for Wafer-Stack Test
- Number of Test Vias & Where
- Existing Standards
- What Test Features

- CPU Core
  - Scan & Debug
  - 1149.1 TAP & Ctrl

- CPU Core
  - Scan & Debug

- Mem Core
  - MBIST

- ASIC Core
  - TempMon
  - Scan
  - 1500 Wrapper
  - Die ID

- DSP Core
  - Scan & Debug
  - LBIST
  - 1500 Wrapper

- FLASH Core
  - MBIST

- 1149/1500 Boundary Scan

- Chip-to-Chip Interconnect Test

- Die-Test Isolation
- Expensive Die & Yield-Loss
- Security & Trust
- New Defect Models

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3D Stack Concerns

- Power-di/dt
- Interposer ^v
- Die Align
- Die Order
- Test Sched
- Access to Each-Die
- Die-2-Die
- Pass Thru
- Boundary Scan
What is being tested?

- There are Chip (IC) Tests
  - Fault Coverage (e.g. Stuck-At, Path Delay, Transition Delay, n-Detect)
  - Defect Coverage (shorts, opens, bridges, GOS)
  - Parametrics (Max FRQ, Leakage – iDDQ, IOH, IIL, VOH, VIL)
  - Functional (Read, Write, Bus Transactions, etc.)
  - Embedded BIST (Logic, Memory, HSIO)

- There are Board Tests
  - PCOLA
  - SOQ
  - FAMI

3D Test is a combination of Both
### Board Test Concerns

#### Structural Devices

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<thead>
<tr>
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<th>P</th>
<th>Presence</th>
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<tbody>
<tr>
<td>C</td>
<td>Correctness</td>
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<td>A</td>
<td>Alignment</td>
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#### Structural Connections

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#### Functional Connections

<table>
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<th>Features</th>
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<tr>
<td>A</td>
<td>At-Speed</td>
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#### Optimizations

| | I | Independent |

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**PCOLA** tests are tests that verify the presence of a chip in a socket or at a board location; that it is the correct chip; and is oriented correctly; receives power and is live; and is aligned correctly.

**SOQ** tests are tests that verify the connections/signals to the chip to be free of shorts and opens; and can assess the quality of the connection's solder joints.

**FAM** tests are tests that can operate or verify a feature of the chip; can be applied at-speed; and that allow a measurement to be taken.

**I** tests are tests that can be operated independently so they can be scheduled in parallel to reduce test time.

Boundary Scan Tests and External Equipment (ICT, X-Ray) and Visual Inspection

Boundary Scan Interconnect Test and X-Ray

Functional Tests

Simultaneous and Concurrent Tests
Use of IEEE Standards?

- 1149.1 is the Base Standard that provides the “protocol”
  - Instruction-Based, Register-Based, Defines the “State-Machine”
  - Defined to assist with Board Test, Described with BSDL/SVF

- 1500 is a derivation used for Core Test
  - Instruction-Based, Register-Based
  - Defined to assist with Cores (Virtual Chips), Described with CTL/STIL

- 1687 is a departure to address certain weaknesses in 1149.1/1500
  - Vectors are defined at the Instrument
  - Mixes Instruction and Data, Defined to assist with Instruments
  - Network-Based (variable length scan paths), Described with ICL/PDL

- 1149.7 can reduce 1149.1’s TAP to just 2 Pins
  - Defines a TDMA packet protocol
Die Access Functions

- Any individual die must provide access functions if applicable
  1. There must be an Access Turn-Around (terminate access at this die)
  2. If there is to be an Upper die (above this die), then there must be an Access Bypass or Access Pass-Through (skip this die without on-die access)
  3. If there is on-chip test/debug logic, then there must be the ability to have On-Die Access
  4. If there is on-chip test/debug logic and an Upper die (above this die), then there must be a combined On-Die Access and a Next-Die Access
Using 1149.1

Instructions:
Up = Next (On-Die-Shared), Bypass, WBR-Upper,
Down = Turnaround, WBR-Lower, On-Die-Only

Assumes next die also has a TAP Controller - so only TAP

No TDI-TDO Strap Needed on Down Instructions

Next-Die Access

Turn-Around
Using 1149.1

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No TDI-TDO Strap Needed on Down Instructions
Using 1149.1

Control Signals must be passed up the stack for non-TAPC die
Using 1500

Next-Die Access

Instructions:
Up = Next, Byp, WBR-Upper, On-Die-Shared, SWIR

Down = Turnaround, WBR-Lower, On-Die-Only

Turn-Around
Using P1687

Top Interface of Die

Turn-Around or Next-Die Access

ab
00 = turnaround (2-bit)
01 = next-die (2-bit bypass)
10 = on-die access only
11 = on-die + next-die access

On-Die Access

Bottom Interface of Die
The Embedded Tester

FPGA Die

Borrow an existing FPGA die to become an Embedded ATE

Download targeted IP instruments to provide stimulus and evaluate responses
FPGA Controlled Test

FCT Tester Coverage:
- GPB coverage
- HSIO coverage
- DDRx coverage
FCT Test Instruments

1. Identify board with FPGA as an opportunity for Embedded ATE
2. Identify Test Goals of Peripheral (PCOLA, SOQ, FAM)
3. Identify needed instruments to meet Test Goals and usage environment (MFG Test, Debug, NPI Test Development, etc.)

Common List of Instruments

1. Pattern Generator
2. Capture Buffer
3. Memory BIST/Test
4. SerDes BERT
5. HSIO Protocols (e.g. PCIe, XAUI, DDRx)
6. SPI/I2C Interfaces
7. D2A Waveform Gen
8. A2D/DSP Sampler
9. Clock Counters
10. Flash Programmer
FCT Methodology

1. Identify board with FPGA as an opportunity for Embedded ATE
2. Identify Test Goals of Peripheral (PCOLA, SOQ, FAM)
3. Identify needed instruments to meet Test Goals and usage environment (MFG Test, Debug, NPI Test Development, etc.)
4. Apply the Embedded Tester Generator:
   - to Create instruments plus IJTAG Network Bit File
   - The tester may support many “Instruments” simultaneously
5. Apply the appropriate tools:
   - Boundary Scan for Interconnect, IJTAG for Instruments, Emulation for Processor
Defining P1687

- **The Controller**
  - 1149.1 TAP & TAP Controller
  - BSDL

- **The P1687 Scan-Path Network**
  - Design-ware, EDA Generated
  - Compliant to P1687 Rules
  - P1687 Network *ICL*

- **The Instrument**
  - IP, Design-ware, EDA Gen
  - Portable/Reusable
  - Raw Instrument *ICL, PDL*

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- **An Architecture [Normative Rules]**

- **Architecture Description (ICL)**

- **Instrument Procedures (PDL)**

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- **Not P1687 is 1149.1**

- **Not P1687 is user IP**

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- **Access Link**

- **ICL Description**

- **PDL Description**

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**SiB**

**TCK**

**TMS**

**TDI**

**TDO**

**TDR**

**RW**

**Done**

**Fail**

**Res**

**Run**

---

**SiB**

**ICL Vectors go here**

**PDL Vectors go here**

---

**Done**

**Fail**

**Res**

**Run**

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Embedding a Tester

Structural Test – Verifies Manufacturing
Performance Test – Verifies Specs

KEY: Have a library of Instrument IP for high demand functions

Complex IP is Test Unit

Compound Complex Instrument

Board Peripheral (BP)

Custom Test Unit (e.g. BIST or BERT)

FPGA Signals-to/from-Peripheral

Original Vectors Here:
Design of IP Incorporates Vectors

Vectors (PDL) retargeted here using IJ TAG-DL

Chip TAP

FPGA

Instrument Vectors (PDL)
P1687 Access to Tester

FPGA

Multiple Instruments can be accessed Simultaneously

Scan Path/Access-Time is fully adjustable by opening and Closing SIBs

Instruments can be started and operated and their SIB access closed down to minimize the scan path length but must be revisited later to collect results

Signal Legend
Blue = Data
Red = Status
Green = ScanPath

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Using P1687 as the OS

Instruments in FPGA

Instrument Operations

Drag & Drop Operations to Schedule Tests

Operations Scheduled as Test Program
Summary-Conclusions

• 3D is one way to extend Moore’s Law
  – We are Stacking Shopping Malls today (not real 3D)
  – 3D comes with many test & debug concerns
  – Solutions must solve both IC Test and Board Test type issues
  – Access is the first item that must be solved
  – The density of functions will be so great that embedding the ATE may be the best solution
  – Similarly, including redundancy and fault-tolerance may be required
  – An ATE can be programmed into any FPGA type logic
  – P1687 enables both the Access and the FPGA Tester OS issues