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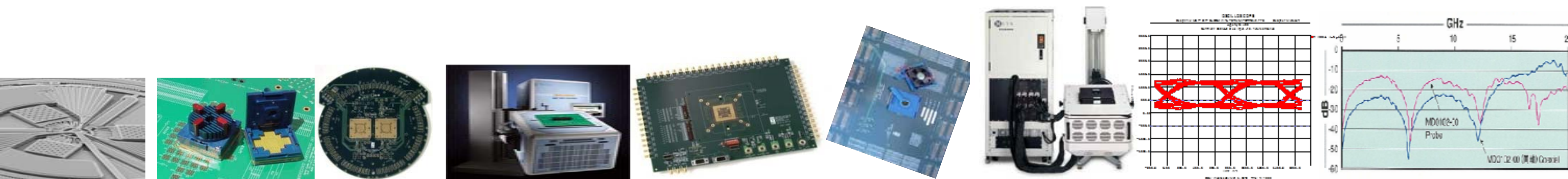

DFT Trends in the More-than-Moore Era

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Mentor Graphics
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Outline

- Semiconductor Technology Trends
- DFT in relation to:
  - Increasing Integration
  - Power Management
  - 3D Packaging
  - Mixed-Signal

Moore's Law
Still A Ways to Go!

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Microprocessor Transistor Counts 1971-2011 & Moore's Law

curve shows transistor count doubling every two years

Transistor count

Date of introduction

Technology Outlook

High Volume Manufacturing	2008	2010	2012	2014	2016	2018	2020	2022
Technology Node (nm)	45	32	22	16	11	8	6	4

Source: Intel

"…rearrange the transistors into a cube and apply the type of advanced manufacturing process expected in 2020, and you'd end up with a processor that occupies about the same volume as a blood cell."

Mile Muller, ARM CTO, October 25, 2011

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Moore is not the end

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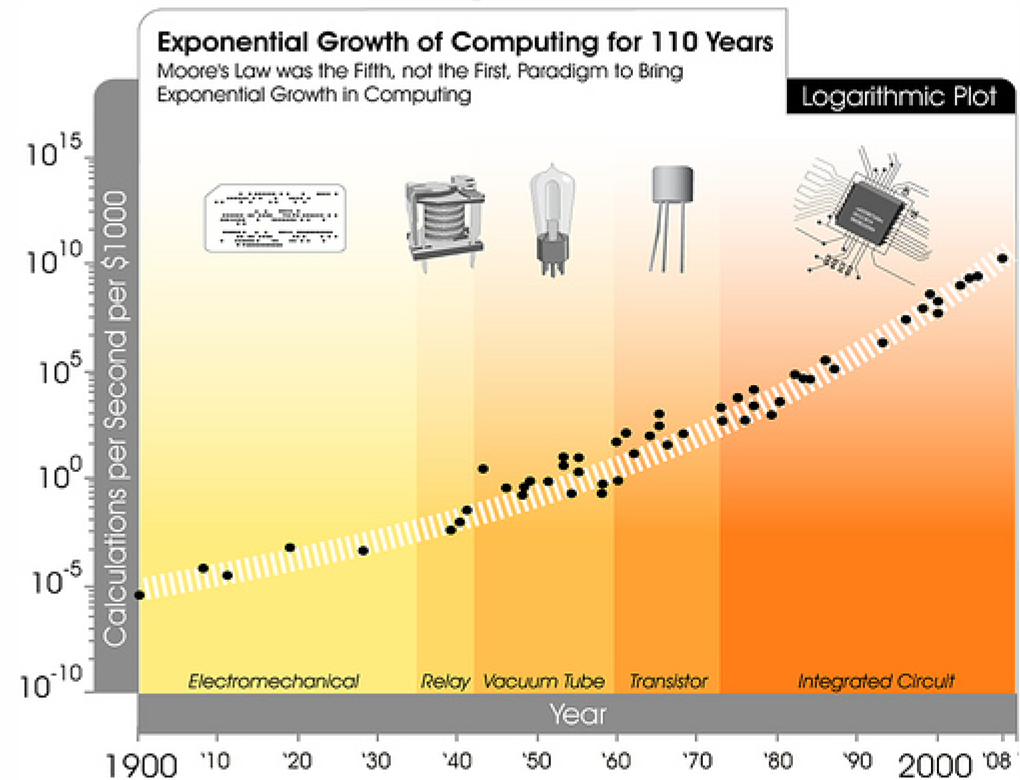
- Exponential growth will continue with next paradigm
  - Graphene
  - Carbon nanotubes
  - Photonics



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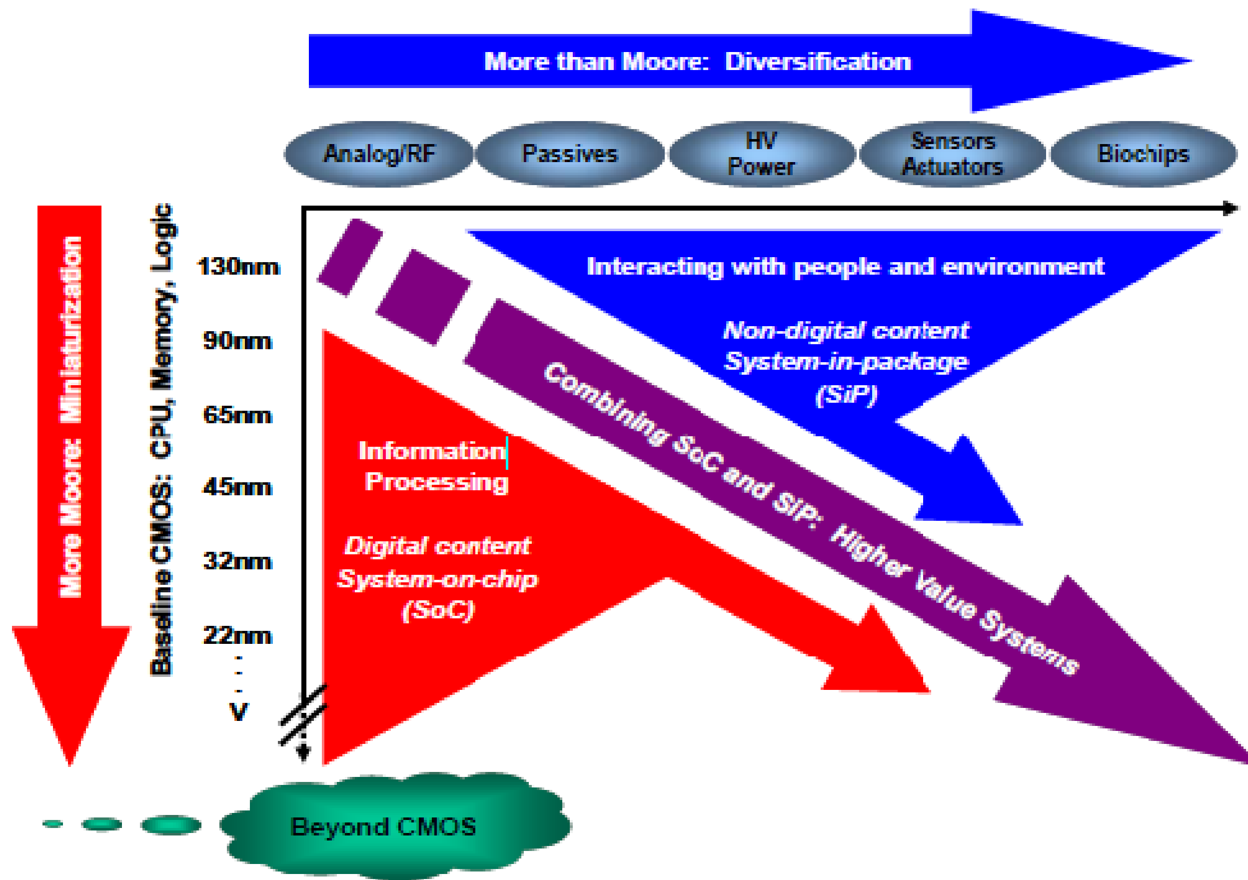
More-Than-Moore



Source: ITRS 2010

DFT in relation to
Increasing Integration

IEEE P1687 - IJTAG
What is it and what is it for?

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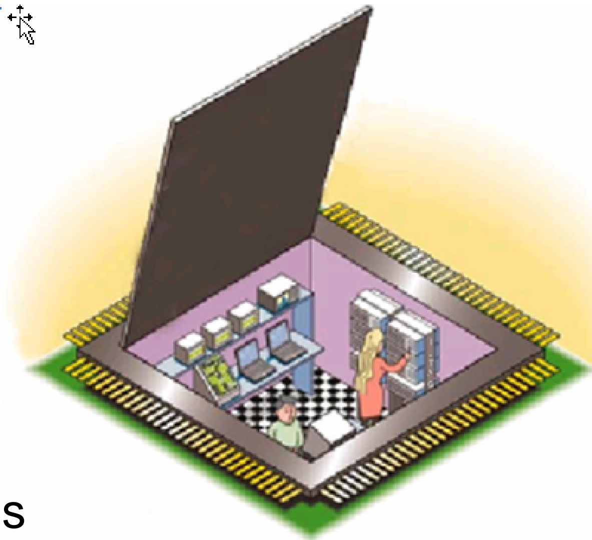
- An IEEE standard proposal
  - Allows plug and play connection and usage (test/debug) of embedded instruments
  - Compatible with 1149.1 but goes well beyond
- Standard includes three main components
  - Hardware rules for 1687 instruments/networks
    - Including port functions, timing & connection rules
  - An Instrument Connection Language (ICL)
    - Describes isolated nodes, partial or complete networks
    - Enables retargeting pin/register reads/writes to scan commands
  - A Pattern Description Language (PDL)
    - Describes instrument usage at a given level
    - Facilitates automatic retargeting to any higher level



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IEEE P1687 At A Glance

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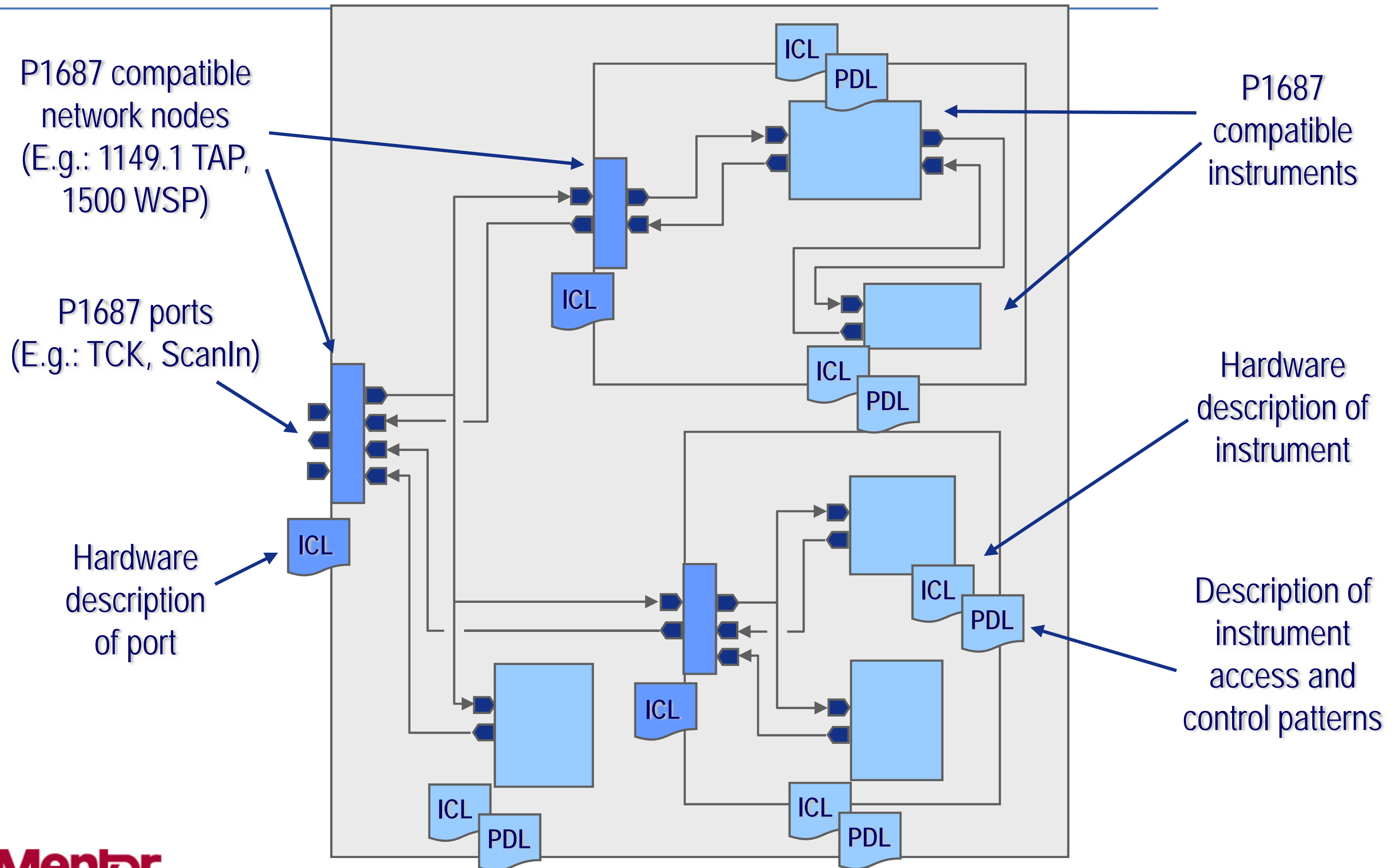

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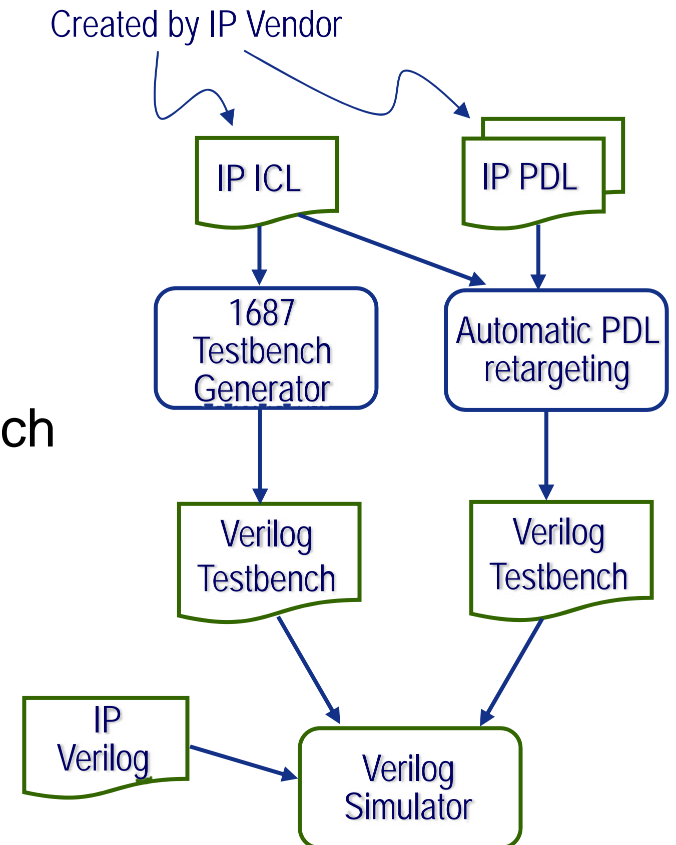
IP IJTAG Certification

- Two new files provided by IP vendor:
  - ICL to describe the IP in isolation
  - PDL routines to describe the IP usage
- Tools incorporated into Tessent
  - ICL reader with automatic verification testbench generation
    - Simulation testbenches
    - ICL visualizers of inferred behavioral model
  - PDL certification and debugging
    - Convert PDL into verilog using ICL description
    - Simulation testbenches to verify IP



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IP IJTAG Integration and Verification

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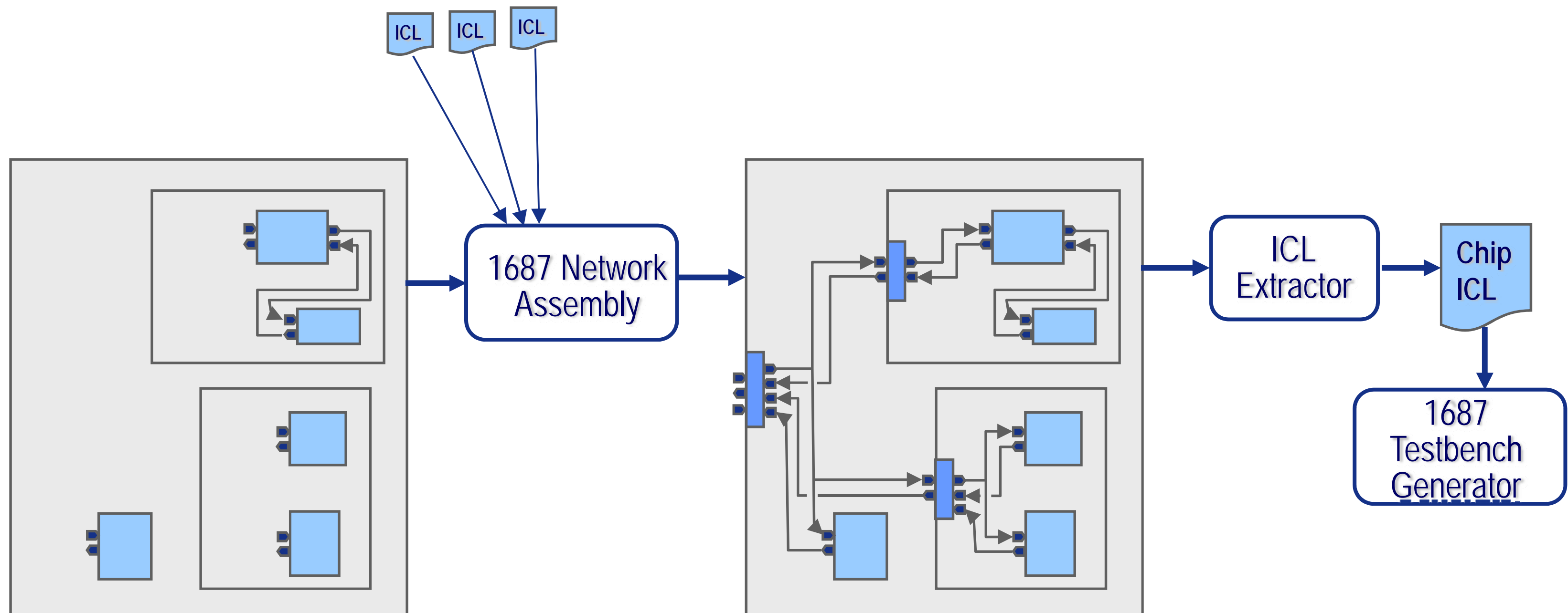
- Integration and verification tools used by Chip Designers / DFT engineers
- Integrates IP instruments and access infrastructure into design
- Create chip level ICL using IP level ICL and RTL/Netlist
- Creates certification testbenches to verify final 1687 network



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Hierarchical Test

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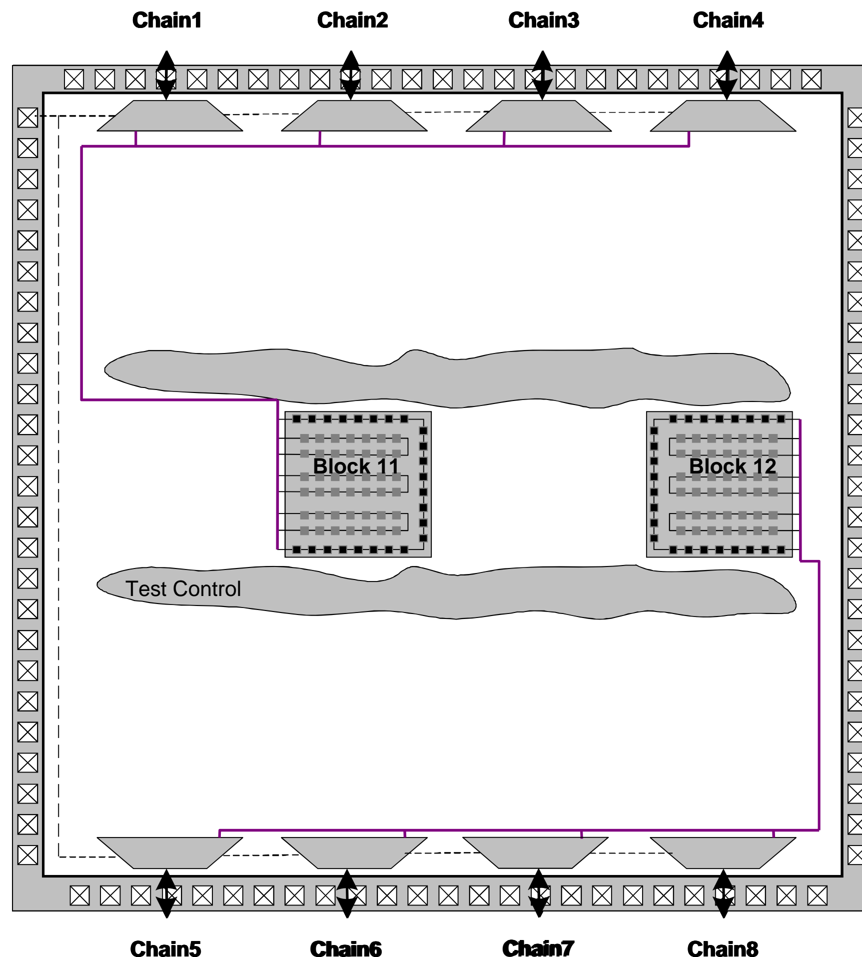
- Critical for handling growing design sizes
- Benefits
  - Reduced memory footprint
  - Reduced tool runtime
  - Core pattern reuse
  - Enables test by region for power management
  - Simplified ECO management

Divide-And-Conquer



- "Blocks" typically correspond to physical design blocks
- Each block isolated by wrapper chains
- Top level sharing & scheduling logic enables testing of blocks in phases with limited I/O

Divide-And-Conquer

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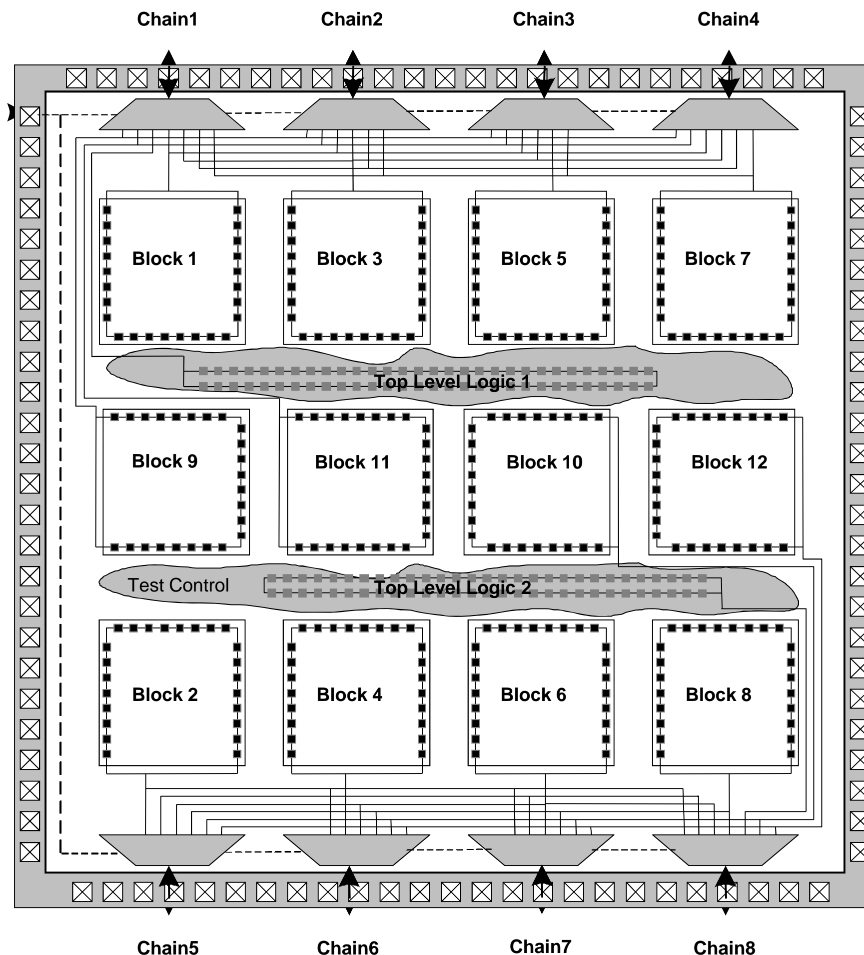
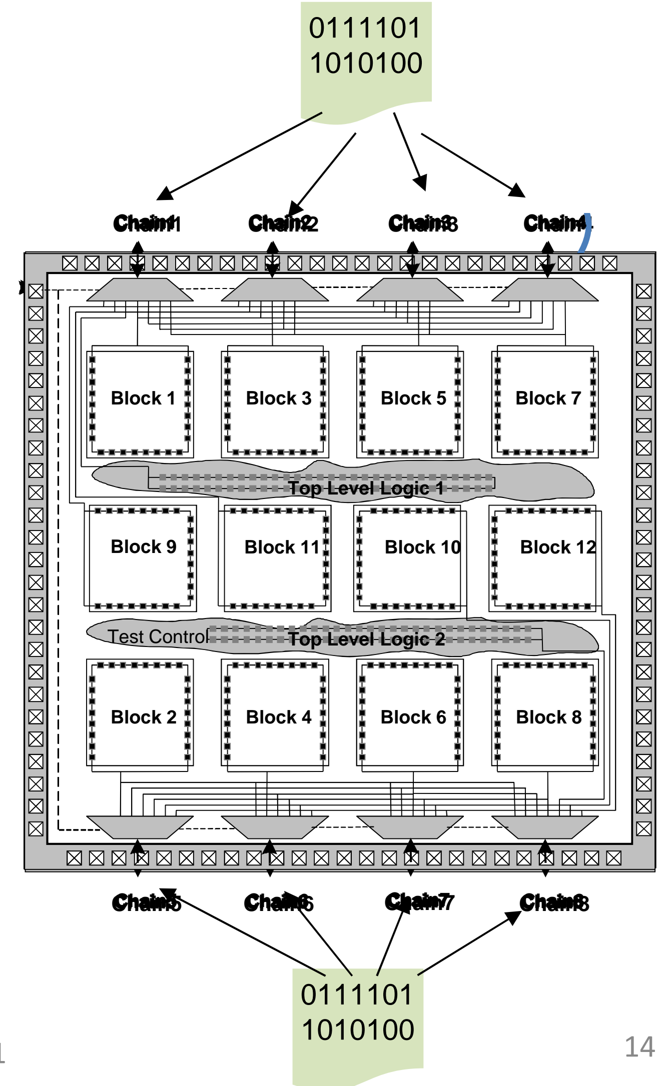


- Blocks configured in External Mode to test top level glue & interconnect
- Only wrapper chains and top level chains needed
- Each block can be represented by graybox

Hierarchical ATPG Flow

1. Core level DFT insertion
2. Core-level ATPG
3. Top-level DFT insertion
4. Core pattern retargeting
5. Top-level ATPG



Hybrid DFT Solution
ATPG Compression and LogicBIST

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- Optimizes defect coverage vs test time
  - Random patterns provide quick basic coverage
  - Top-up compressed patterns efficiently complete coverage
- Reduces test pattern volume
- Reduces test pattern generation time
- Provides key optimizations between parallel and serial test applications

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Hybrid DFT Solution
Core test times

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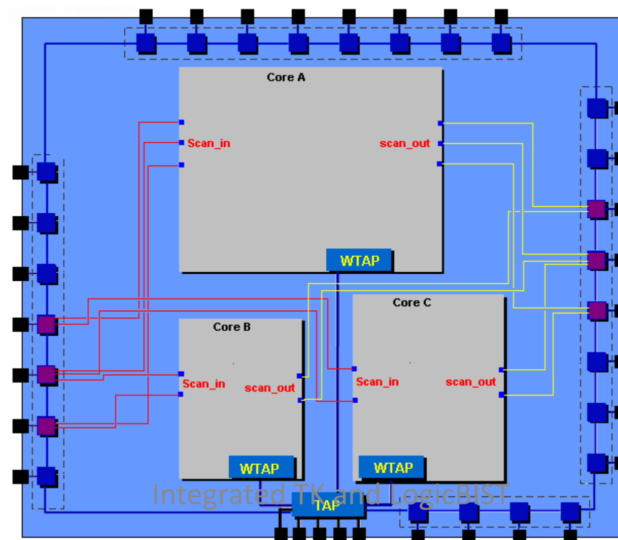
Core A	TK test-time (ms)	LBIST test-time (ms)	total coverage (%)	total test time (ms)
Hybrid (LBIST and ATPG)	156	160	99.6	**316**
TestKompress (ATPG ONLY)	460	0	99.55	460

Core B	TK test-time (ms)	LBIST test-time (ms)	total coverage (%)	total test time (ms)
Hybrid (LBIST and ATPG)	110	216	99.45	326
TestKompress (ATPG ONLY)	250	0	99.4	**250**

Core C	TK test-time (ms)	LBIST test-time (ms)	total coverage (%)	total test time (ms)
Hybrid (LBIST and ATPG)	100	199	99.7	299
TestKompress (ATPG ONLY)	240	0	99.65	**240**



Integrated TK and LogicBIST

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Hybrid DFT Solution
Test Time Optimization

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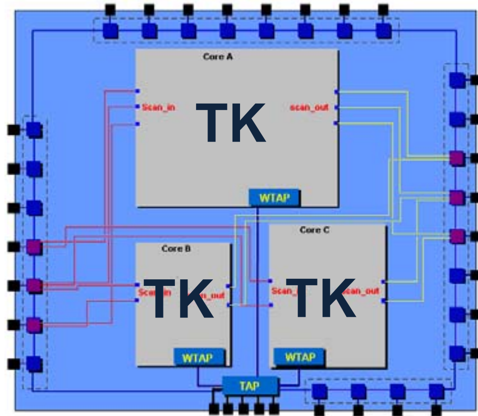
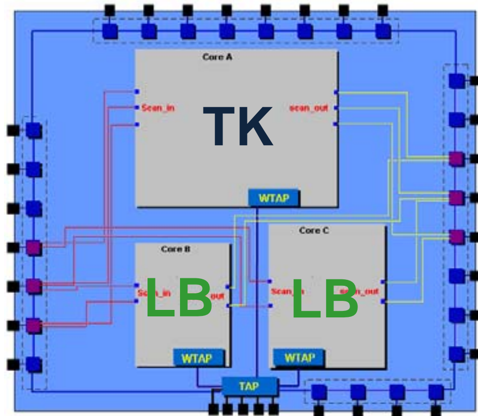


Test Time = 460 + 250+ 240 = 950



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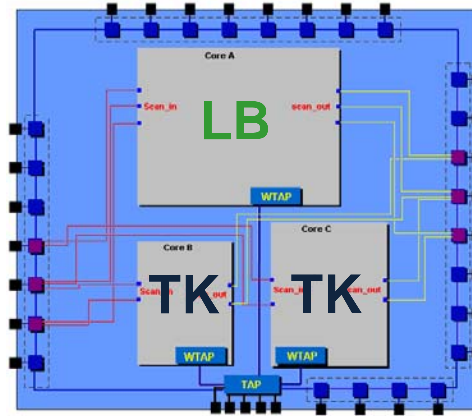

Test Time =

Max(156, 216, 199) +
Max(160, 110+100)

= 216 + 220 = 436

DFT in relation to Power Management

Growing Power Challenges

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- Not only for growing number of mobile devices …

- … but for all electronics including computing

Apple Solar Farm To Power North Carolina Data Center

First Posted: 10/29/11 08:45 PM ET | Updated: 10/29/11 08:48 PM ET

React > Inspiring | Enlightening | Infuriating | Scary | Helpful | Amazing | Innovative | Adorable

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Apple is reportedly increasing their investment in renewable energy, according to *The Charlotte Observer*. Apple was recently issued the necessary

Power introduces Unique Challenges

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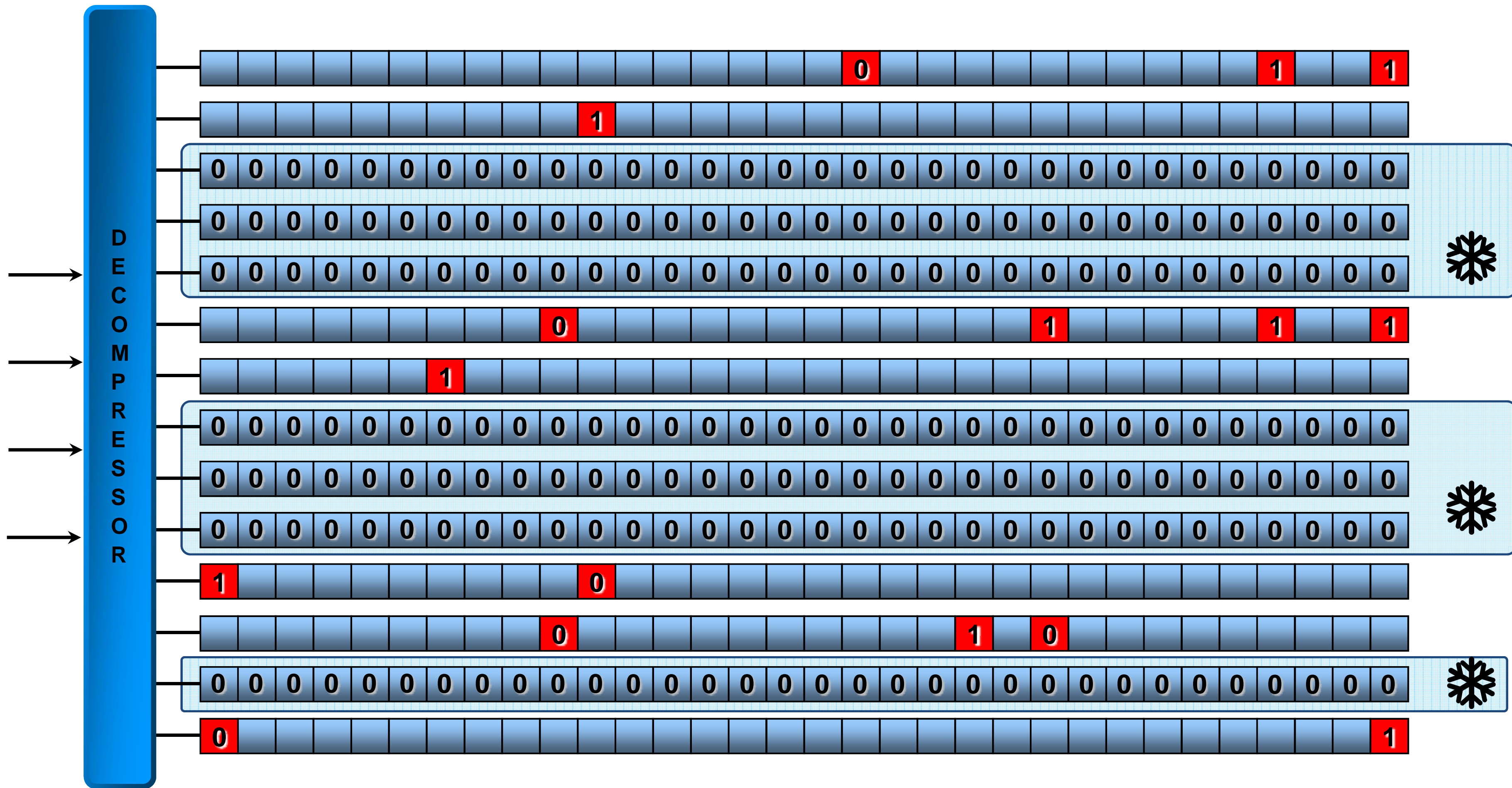
- Design teams adopting new techniques for power management
  - Power gating
  - Retention and isolation cells
  - Dynamic voltage & frequency scaling (DVFS)
- Power-aware testing techniques required
  - Low-power ATPG
  - Low-power LogicBIST
  - Power-aware test generation

Low-Power Decompressor

Reducing Switching Activity During Shift



Load/Response Shift Switching Activity

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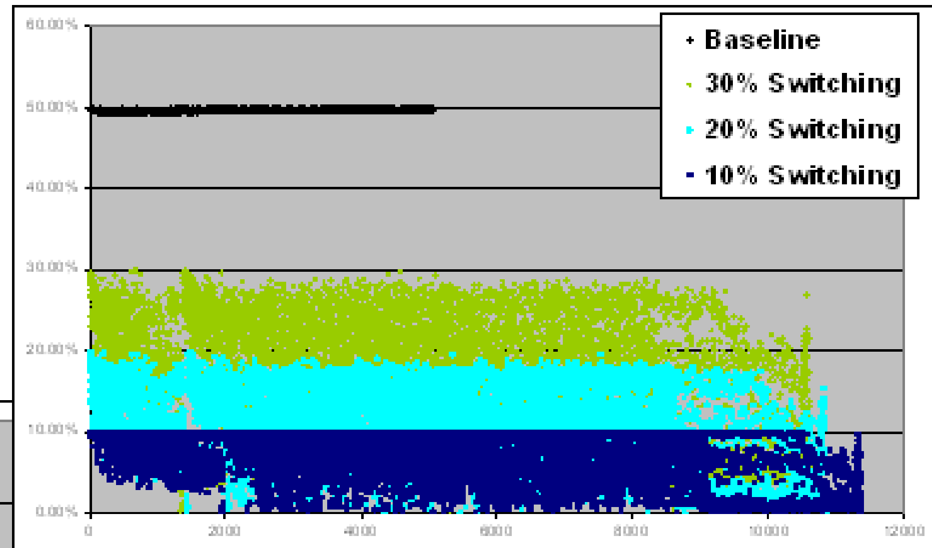
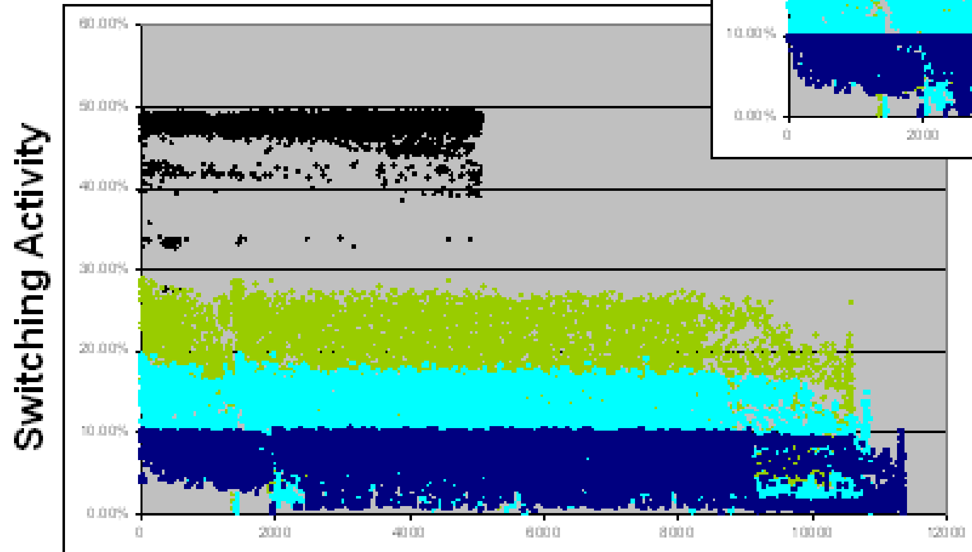
Load Shift



Response Shift



Pattern Number

Notes:

- Switching threshold met without coverage loss
- Reasonable pattern increase while maintaining coverage

Low-Power LogicBIST

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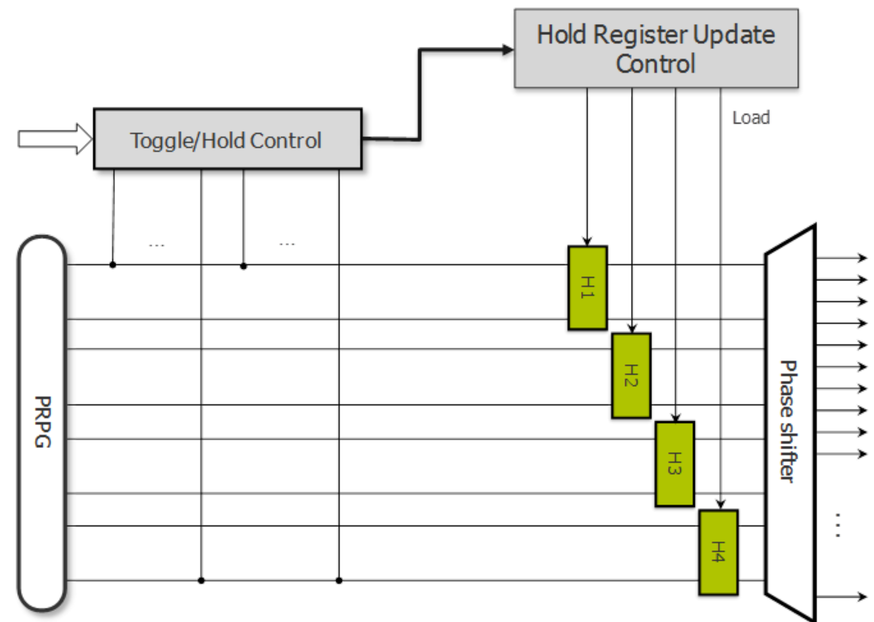
- Reduces both shift and capture power
- Minimal or no impact on test coverage
  - Recover coverage by increasing pattern count
- Allows optimization between switching activity and pattern count
- Minimal silicon area overhead



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Low-Power LogicBIST Typical Results

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Hold Regs	Toggle Prob. Regs	Hold Prob. Regs	# patterns	Effective patterns	TC (%)	Load Toggle	Unload Toggle
Conventional LBIST			10,000	1,849	85.12	49.84	48.69
4	3	2	10,000	2,018	84.52	26.15	27.51
			11,392	2,189	85.15	26.13	27.75
4	2	2	10,000	2,041	82.18	17.50	19.77
			17,856	3,006	85.12	17.49	20.14
4	2	3	10,000	2,107	79.68	10.90	13.82
			29,952	4,397	85.12	10.93	14.53
8	3	3	10,000	2,068	78.44	9.23	12.31
			33,344	4,771	85.12	9.23	13.53

Design: 1.4M gates, Scan config: 160 x 541

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Power-Aware Test Generation

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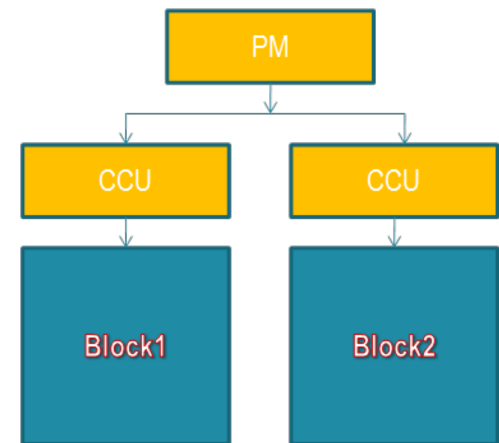
- Test sequence automation for multiple power states
- Test of low-power components
  - Level-shifters: test under difference voltage corners
  - Retention cells: test with source domain on then off
- DFVS support
  - Need to run tests at all legal voltage and frequency combinations

		Power domain		
		1	2	3
Power state	A	Off	On	On
	B	On	Off	On
	C	On	On	Off



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DFT in relation to 3D Packaging

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Why 3D-IC?

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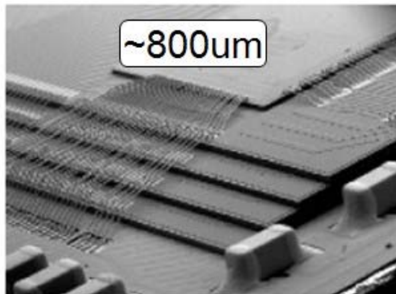
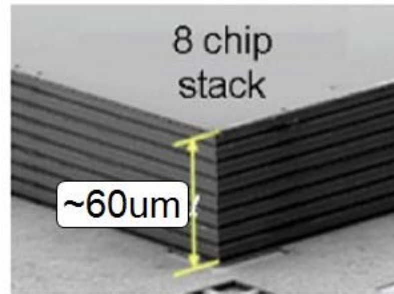
- Performance
  - High bandwidth / bus width interfaces
    - GPU/CPU devices
    - Memory
    - Overcome wire-bond “performance wall”
  - Lower power
    - Shorter wires / connections
    - Eliminates high voltage/power I/O drivers
- Form factor
  - Smaller, superior product
    - CMOS Image Sensor
    - Memory
    - Memory on logic

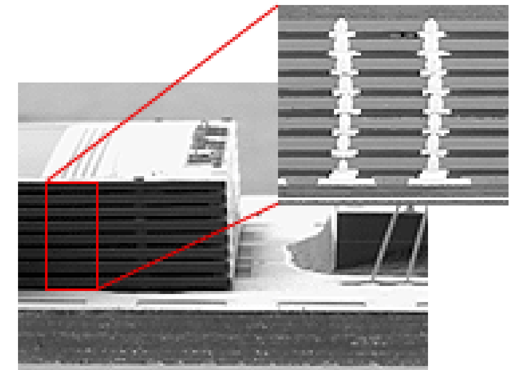


Stacked, Wire bonded IC’s



3D-IC with TSV*

Through Silicon Via



Samsung 8GB DDR3 DRAM

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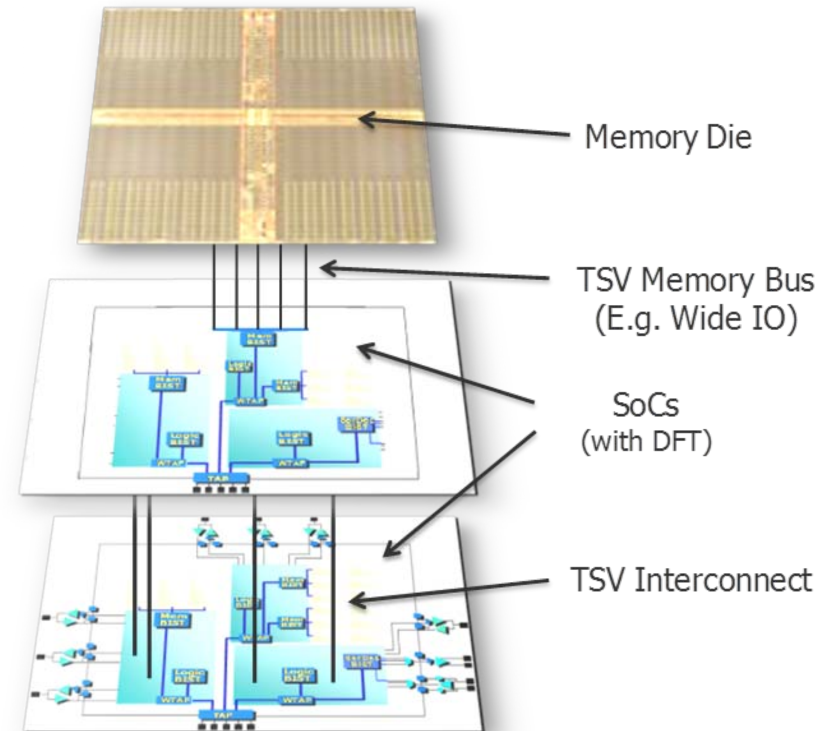
3D Test Assumptions

- DUT assumed to be stacked die with TSV connections
  - Any number and combination of memory and logic die
- Some form of access to test resources within each die available
  - E.g. IEEE P1838 and/or IEEE P1687
- Test objectives
  - Test TSVs between logic die
  - Test TSVs between logic and memory



Logic-to-Logic TSV Interconnect Test

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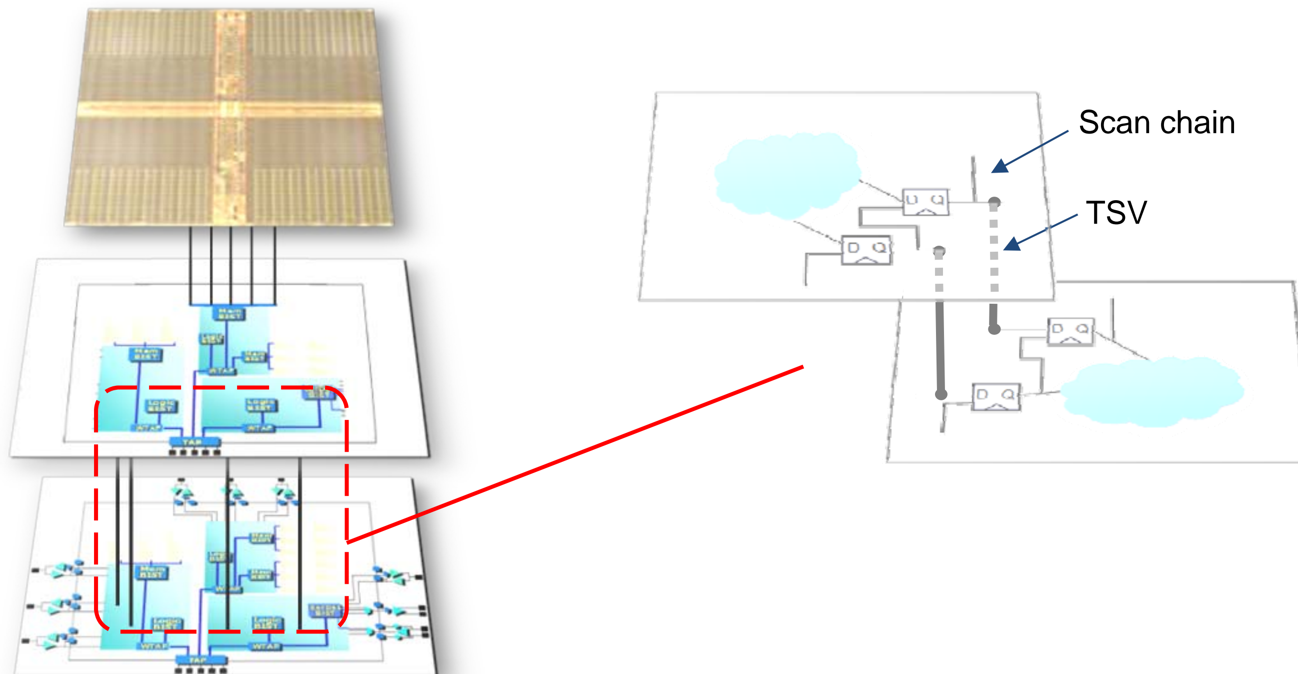

- TSVs covered by hierarchical test approach
  - TSVs between scan-isolated cores on neighboring die
  - Any supported fault models can be used

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Stacked Memory Test

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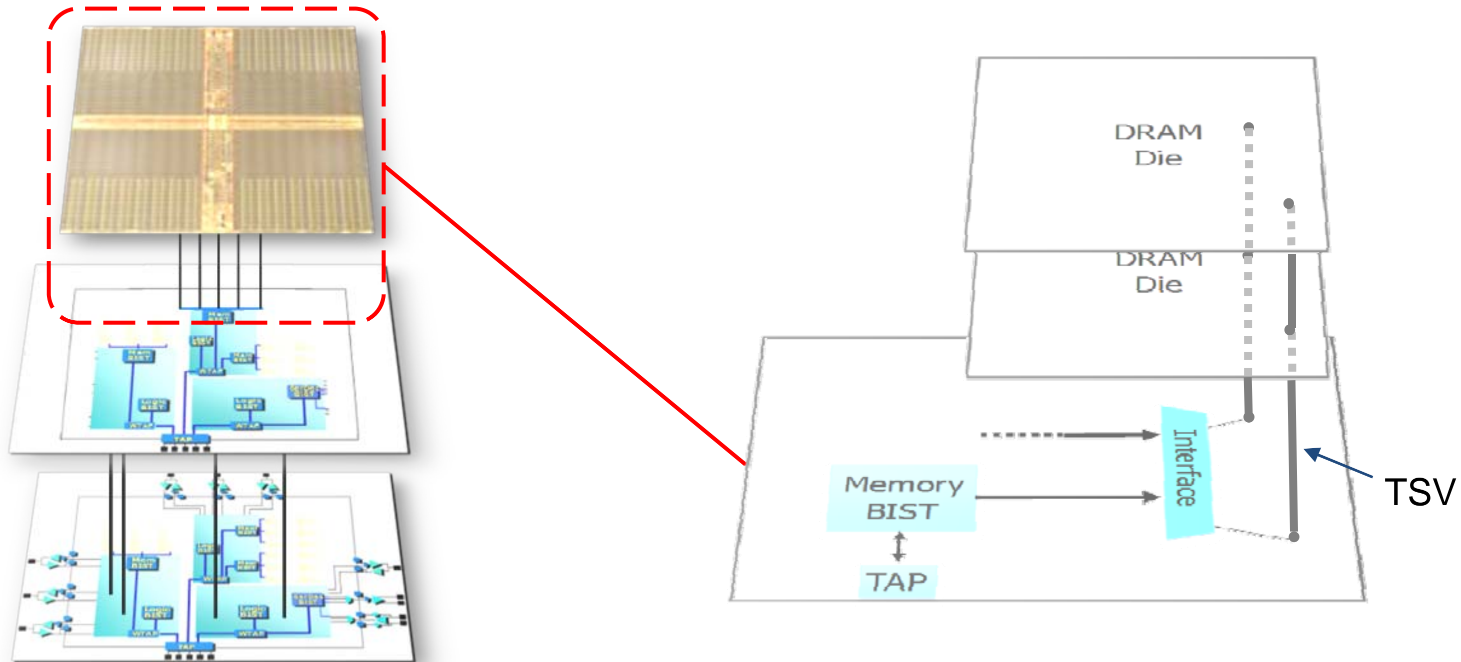

- External Memory BIST added to logic die
  - Provides full-speed testing of memory die and bus
- *Shared-bus* capability supports multiple external memory die
- Post-silicon programmability supports changes in memory die

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DFT in relation to Mixed-Signal

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Mixed-Signal Test
Growing Challenge!

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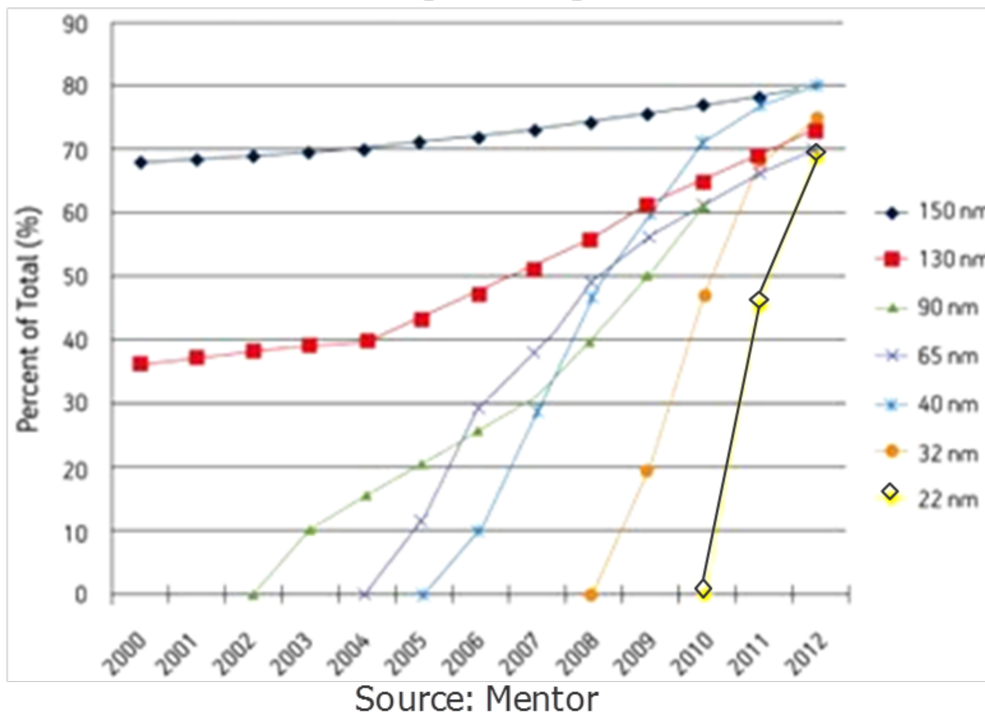
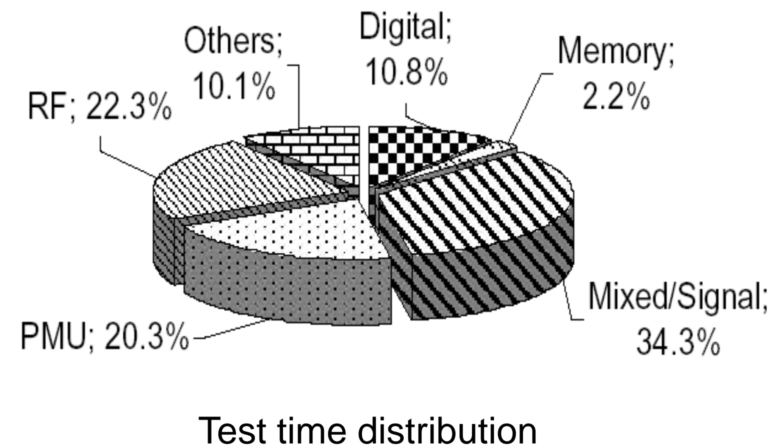


Source: Mentor



Test time distribution

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Mixed-Signal DFT
Where are we at?

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PLL

SerDes

DDR I/Os

Comprehensive commercial BIST solutions available

Digital solutions provide pico-second accurate measurements

ADC/DAC

Some DFT and BIST techniques available

Solutions still generally too slow and/or not general enough

Analog

General BIST solution under development
Simple DAC/ADCs used to convert to digital domain
Defining analog fault models

RF

Limited to monitor buses

Summary

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- More-than-Moore era will continue to push design and test for the foreseeable future
- DFT evolving on multiple fronts
- Highly scalable solutions are a must
- Next major challenges are 3D and mixed-signal