



# Agenda

- 
- Customer requirement
  - Characterizing memory controllers
  - HSMI solution
  - Project rollup, Conclusion



# Customer requirement

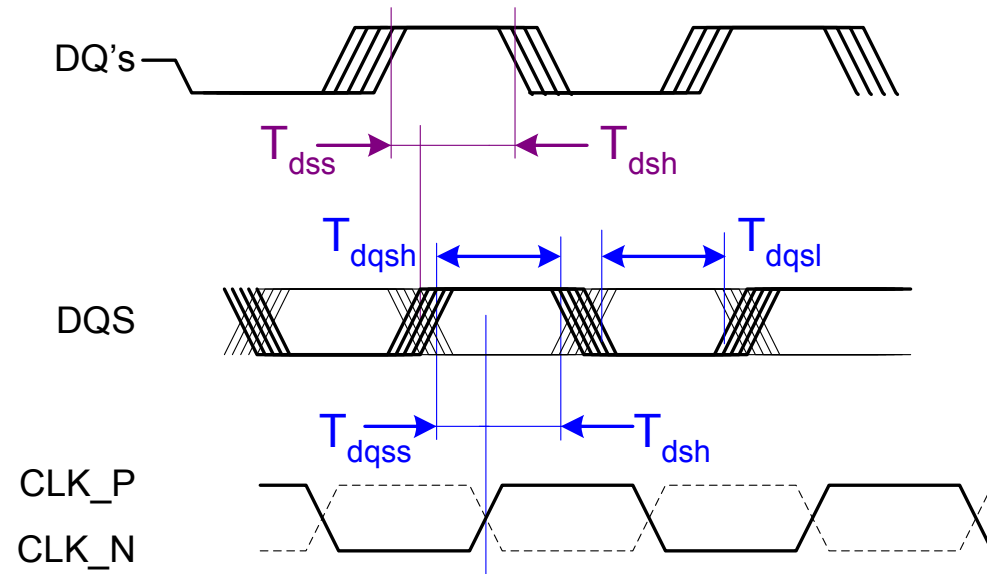
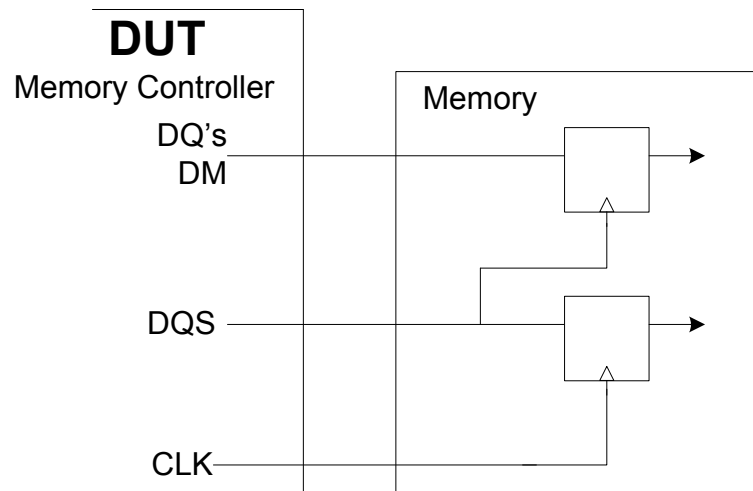
- Large majority of processors and SOC devices are interfacing with DDR2/3 memories through 1 or multiple embedded memory controllers
- DEFT is commonly used to check controller functionality, however, functionality and Physical layer verification still requires Source sync ATE and/or strobe alignment prior to testing
- In order to characterize precisely a SOC product line using a DDR3 interface and monitor its process, a customer wants to perform statistics on High Speed Memory Interface and gather Key parameters.



# Characterizing memory controllers

## Memory requirement and DUT model

### Write cycles:



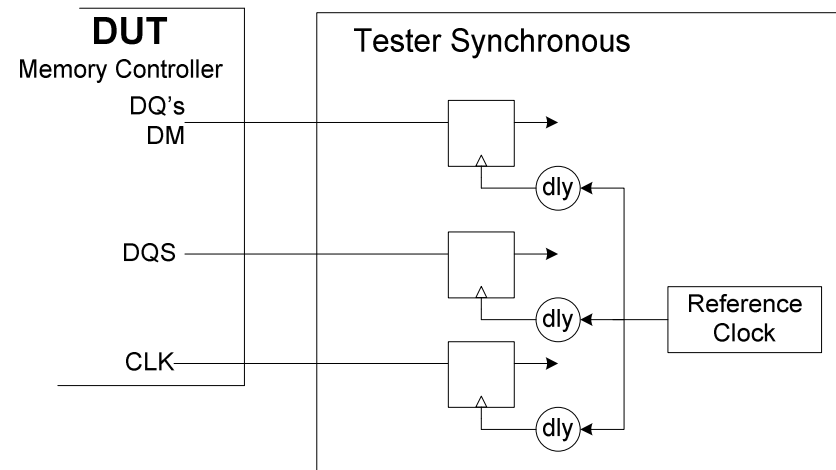
# Characterizing memory controllers

## $T_{dqsh}$ evaluation using Tester Synchronous ATE



- Clocks are typically generated from DUT internal PLL/DLL. Tco is unknown
- Before performing any functional test, a timing search is performed to find out where the clock seats. DQS, DQ timing are then set accordingly.

- 2 timing search are necessary to get  $T_{dqsh}$
- System and device Jitter is such that getting  $T_{dqsh}$  precisely is almost impossible

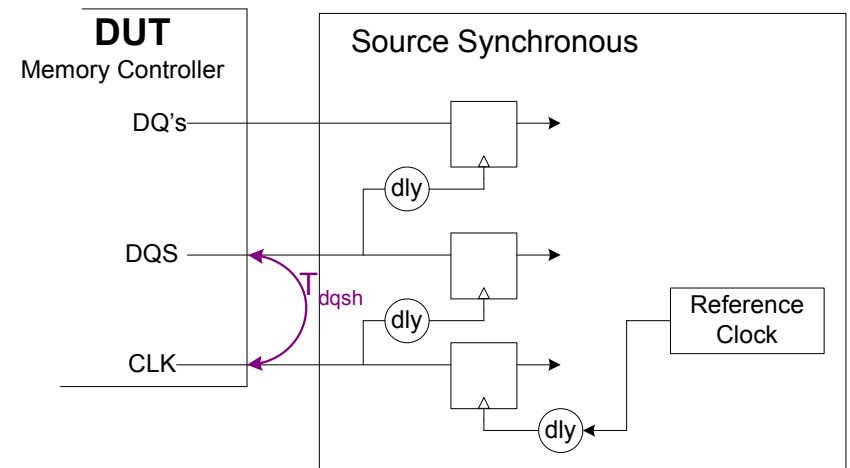


# Characterizing memory controllers

## $T_{dqsh}$ evaluation using Source Synchronous ATE



- Tco is still unknown, but not an issue anymore
- Functional test can be performed on Dqs as long as Delay line are set properly
- 1 timing search is necessary to get  $T_{dqsh}$



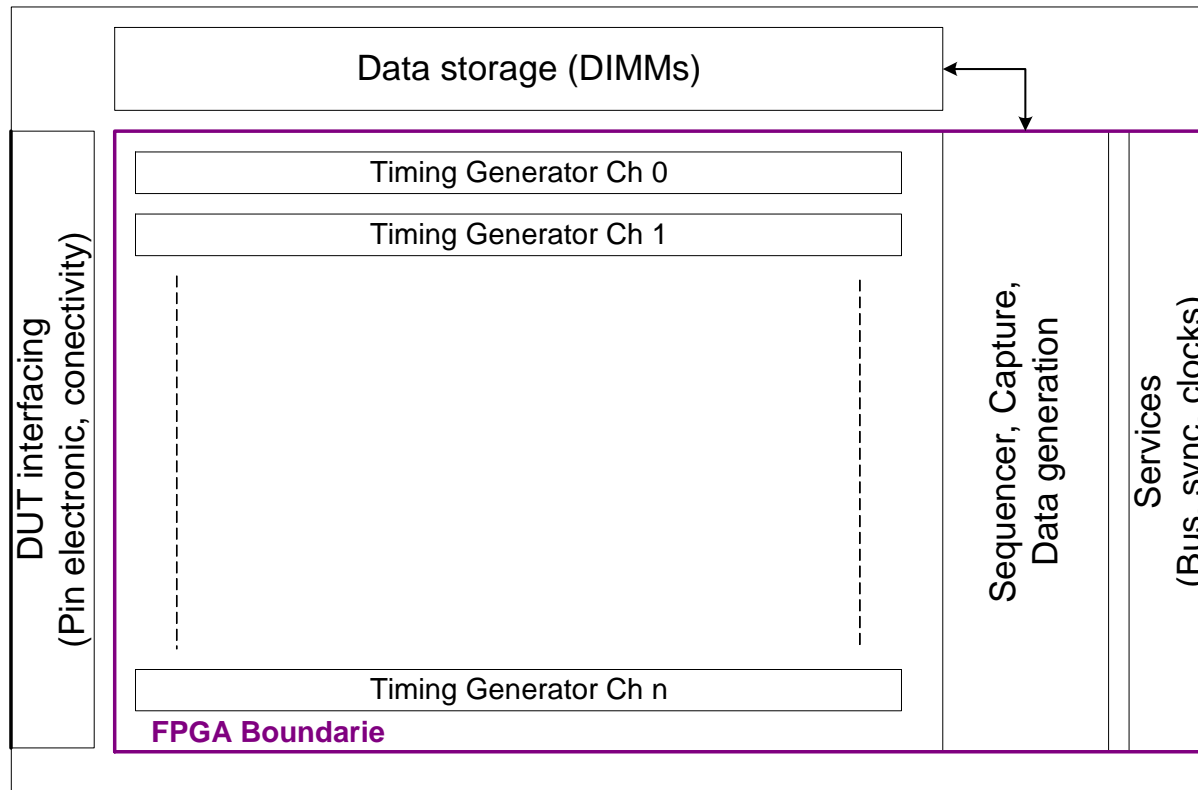
- **Tester Synchronous** solution does meet the timing accuracy requirement
- In addition to its costs, **Source Synchronous** tester requires too much time. Statistics on 1000 search requires in the order of  $1000 \times 100\mu\text{s} \times 30$  steps = 3 s per parameters

→ Dedicated solution is required



# HSMI Solution

## Technical implementation



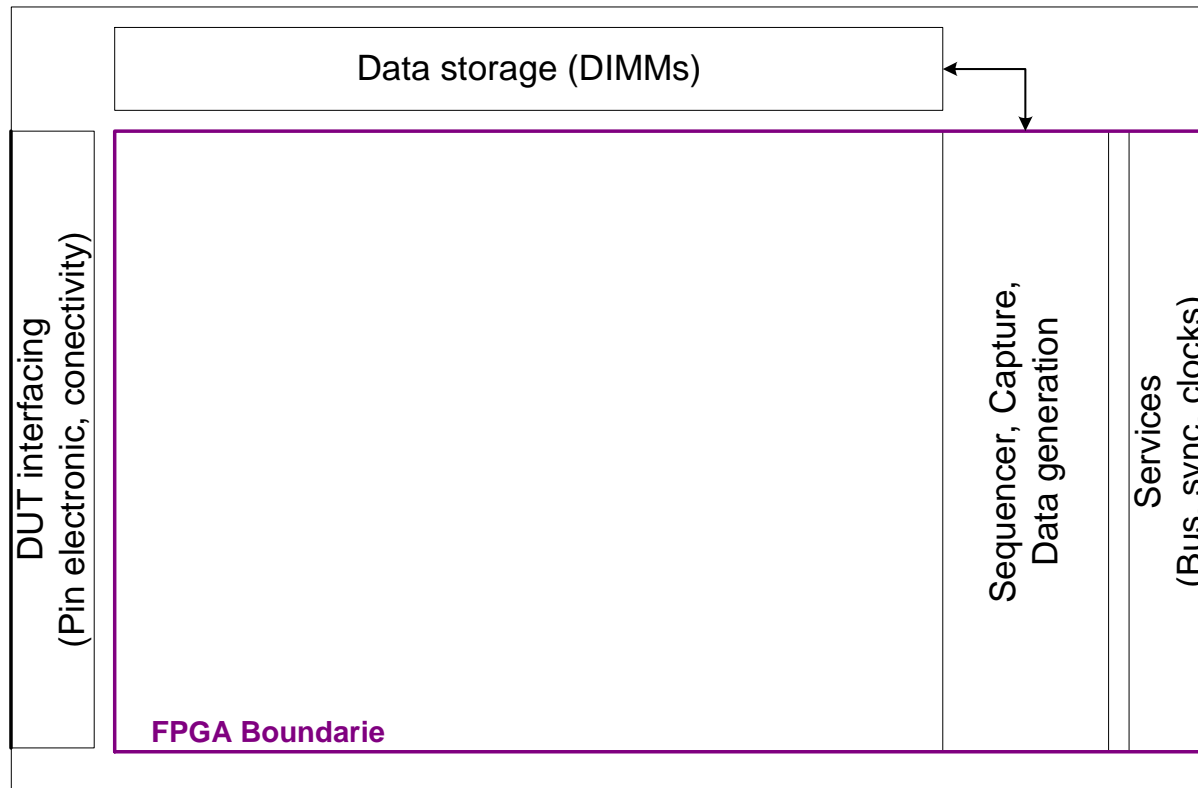
- Start from existing instrument (HW/FW)
- Remove timing generators
- Implement new FW
  - SS capability
  - Automatic cycle type detection
  - $\Phi(\text{clk}, \text{ctrl})$  capability
  - $\Phi(\text{clk}, \text{dqs})$  capability
  - $\Phi(\text{dqs}, \text{dq's})$  capability

- Dedicated search & statistics within FPGA



# HSMI Solution

## Technical implementation



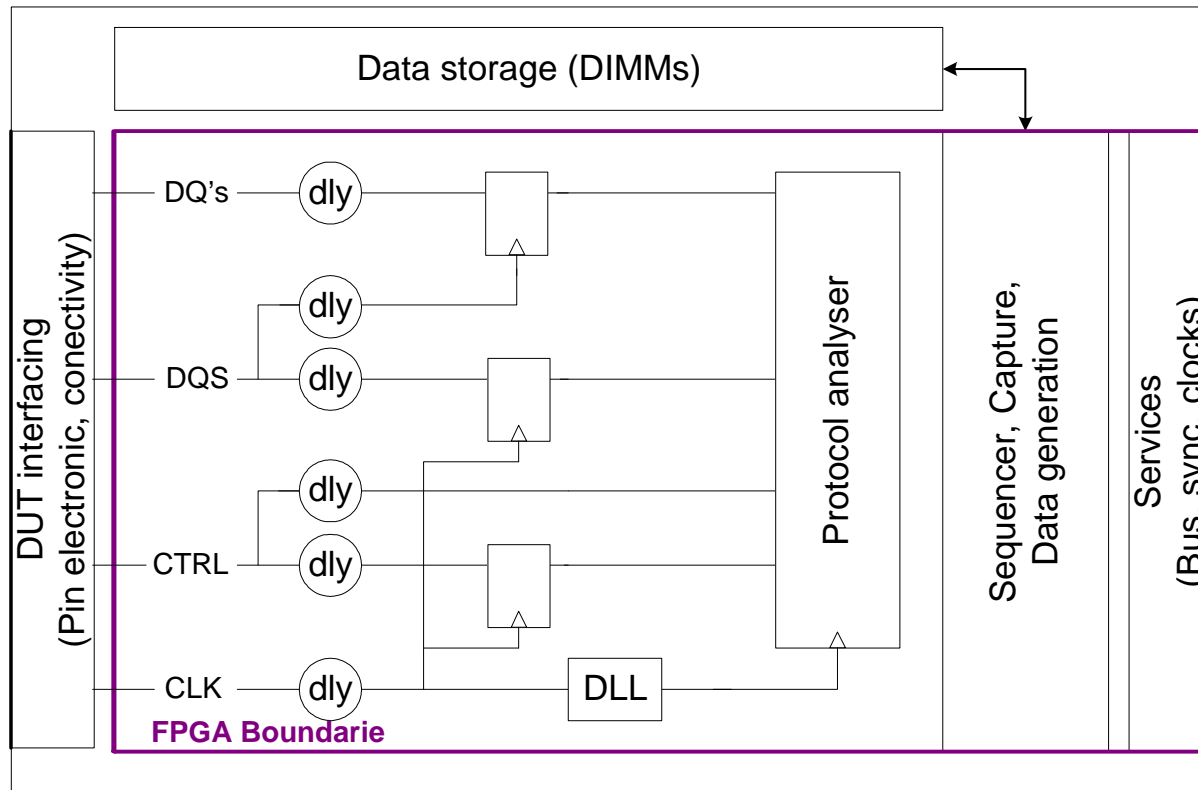
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## Technical implementation



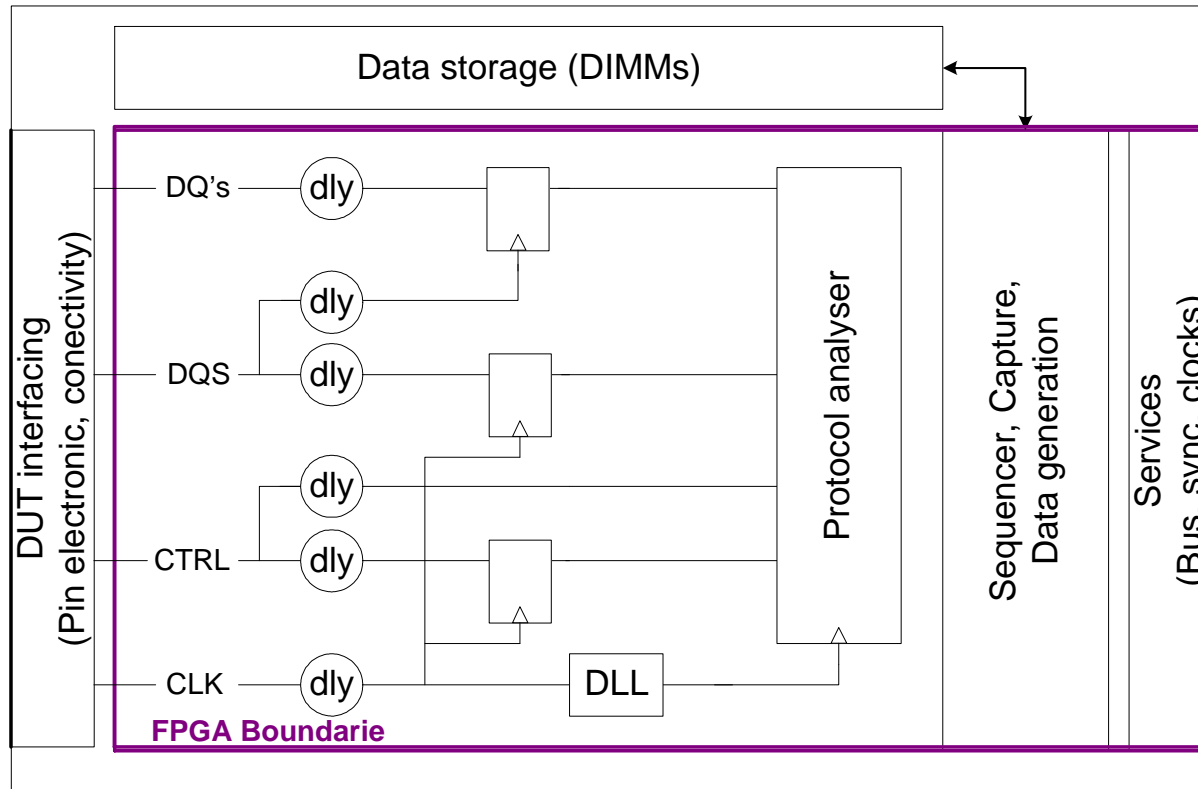
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# HSMI Solution

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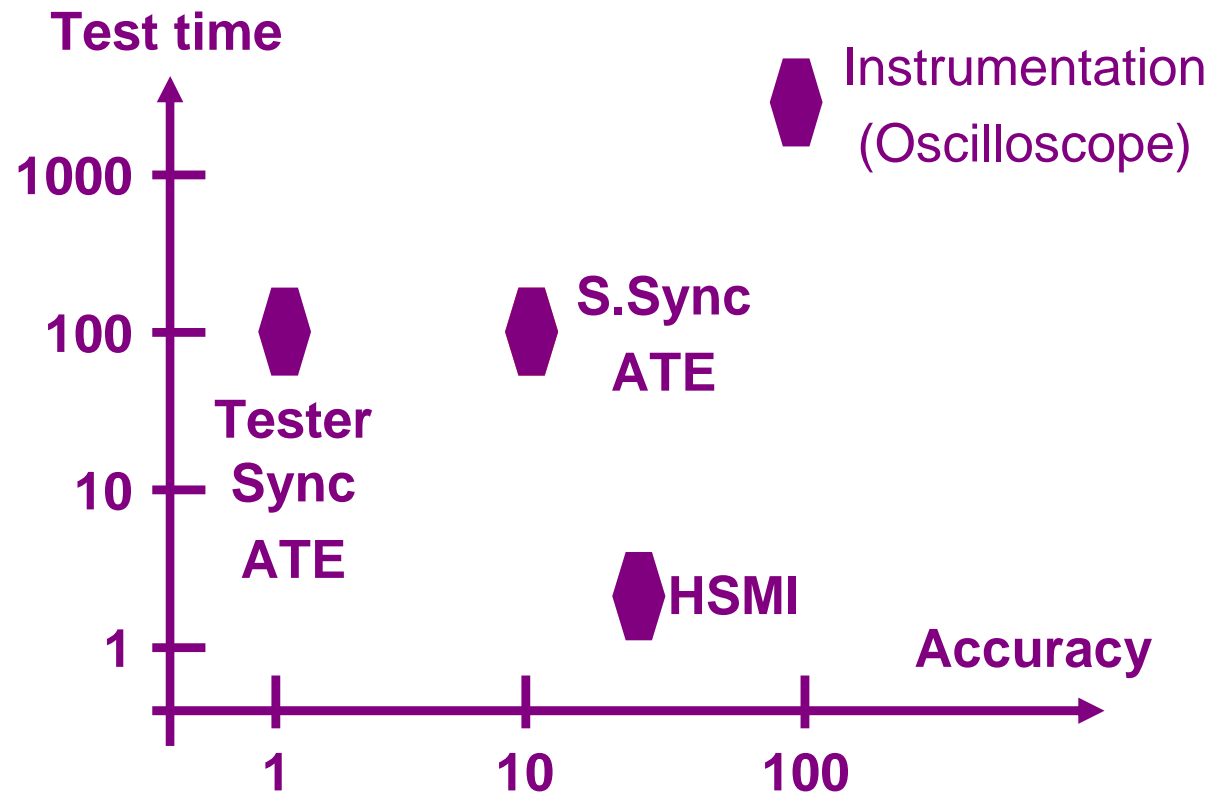
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- Measure, characterize HSMI physical layer key parameters in less than 100ms

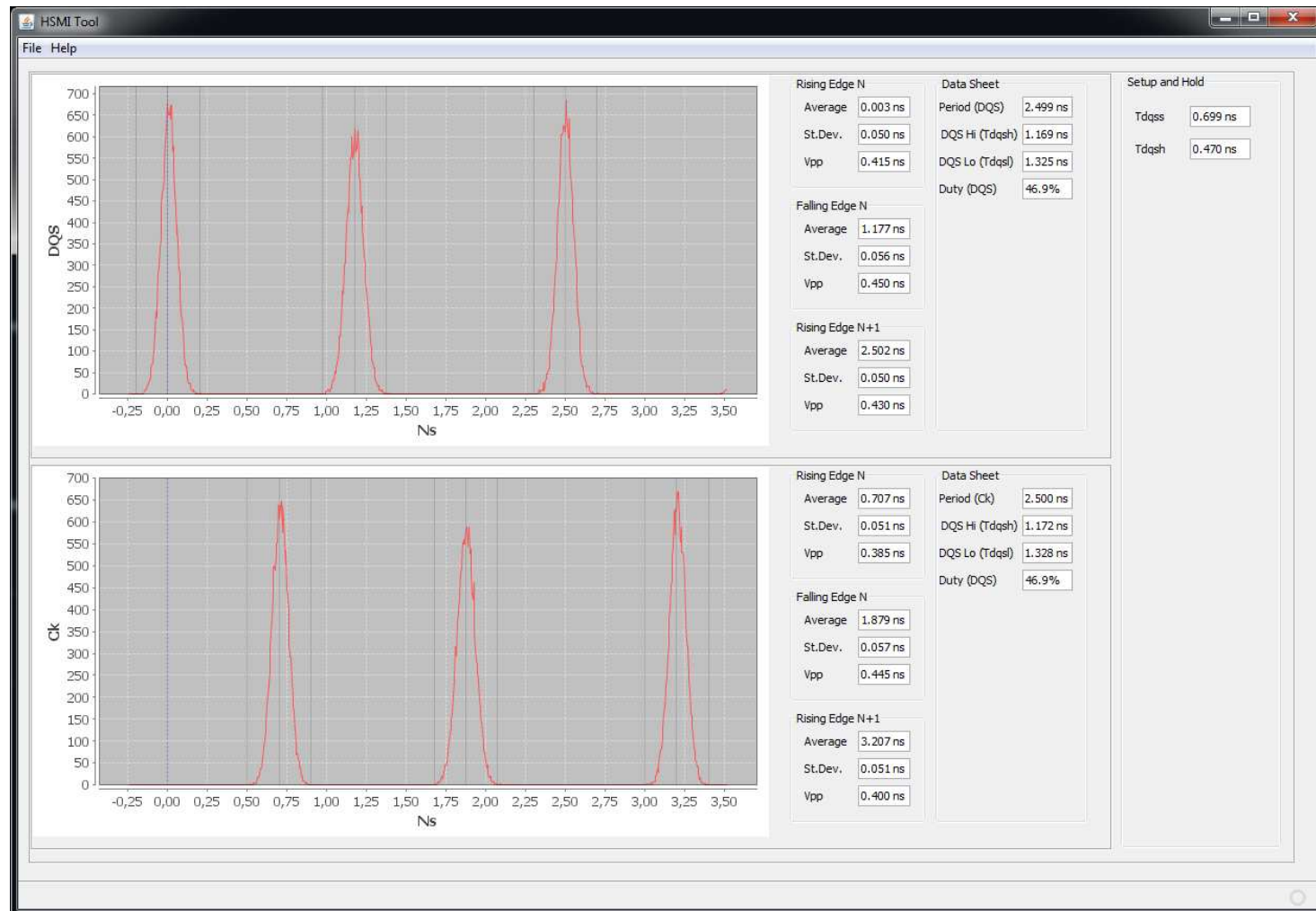
- $T_{DQSS}$ ,  $T_{DSS/H}$ ,
- $T_{DSS}$ ,
- $T_{DQSH}$ ,  $T_{DQSL}$ ,
- $T_{DS}$ ,
- $T_{DH}$ ,
- $T_{DQSCK}$ ,
- $T_{DQSQ}$  ...



# HSMI Solution

## Key features

- Engineering/debug environment providing help for analysis.



# HSMI Solution

## key project comparison

|                                     | FPGA Based instrument | Dedicated new instrument |
|-------------------------------------|-----------------------|--------------------------|
| From requirement to proven solution |                       |                          |
| - Duration                          | 4 months              | ~ 15 months              |
| - Effort                            | 8 pers. months        | 24 to 50+ pers. month    |
| Development cost                    |                       |                          |
| - Labor                             | \$80K                 | \$250K to \$3 000K       |
| - prototyping                       | -                     | >> \$100K                |
| - Validation tooling                | \$20K                 | \$20K                    |
| Return On Investment                | 2 systems             | 10 systems               |



# Project Roll up - Conclusion

- Density and functionalities embedded in modern FPGA enable building of wide variety of ATE instruments, from production to characterization systems
- Furthermore, re configurability, development cost and cycle time make them perfect candidate to answer the increasing needs for dedicated solutions.



Thanks  
for your attention

