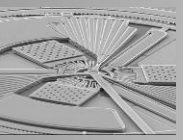
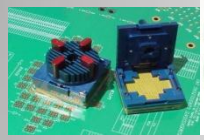
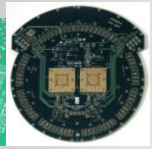




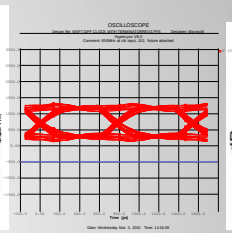

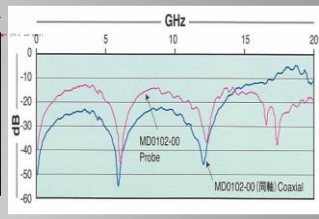

A Fine Pitch MEMS Probe Card with Built in Active Device for 3D IC Test

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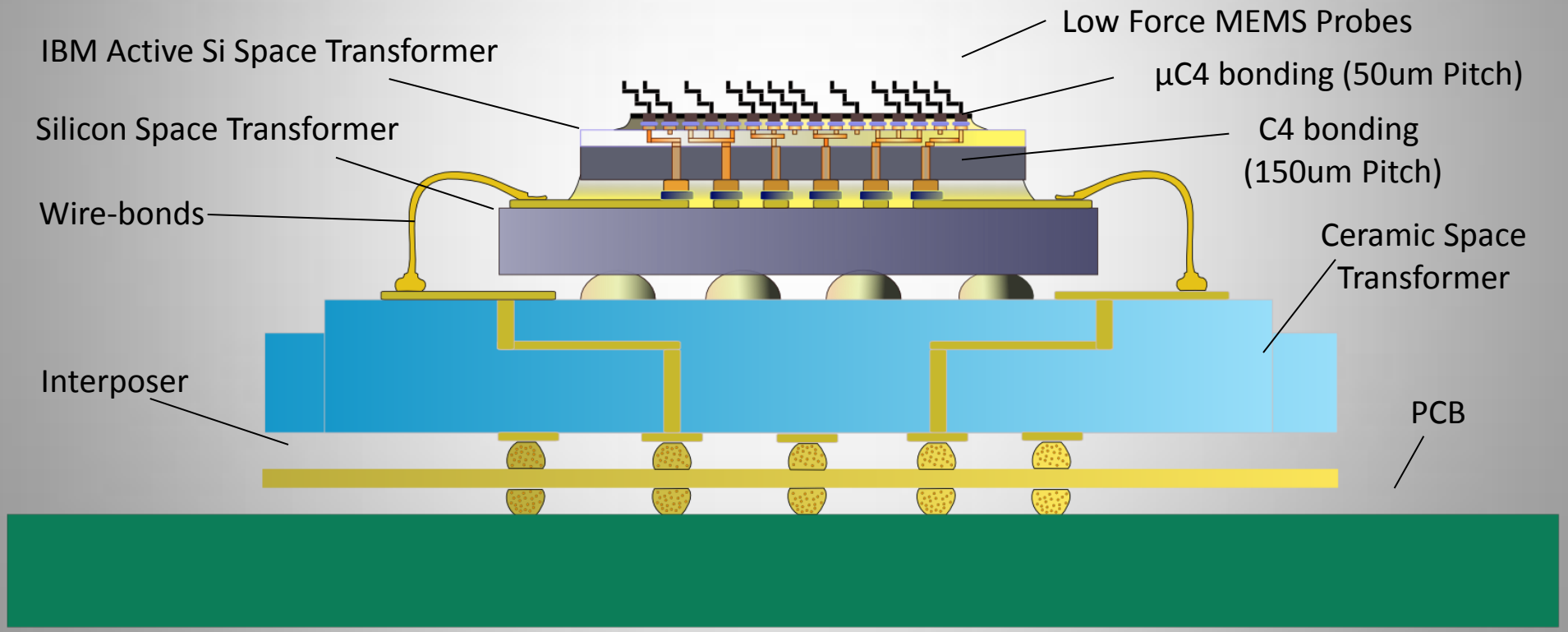
Overview

Silicon Valley Test Workshop

- Probe Card Architecture
- 3D Silicon Technology: Role of Test
- Probing Challenges & Benefits of Active Probe Card
- The Probing Solution
- Test Results
- Summary
- Acknowledgements

Active MEMS Probe Card Architecture



Active MEMS Probe Card Challenges and Benefits

Silicon Valley Test Workshop

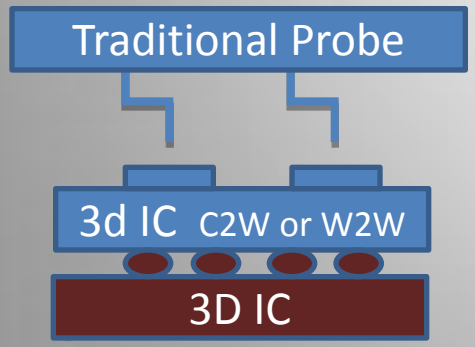
- Examples of current / future Challenges
  - Silicon and Packaging Technology Scaling
  - New Test Insertions and More Test Partitioning
- Benefits of using an Active Probe Card
  - Mitigate Rising Cost of Test (COT)
  - Extend ATE and Bench Instrumentation
  - Inter-strata In-Out (ISIO) Buffering / Performance Testing
  - Chip to Probe Centric Design for Test (DFT)

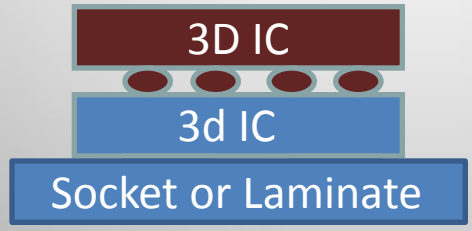
3D Silicon Technology : Test then Stack

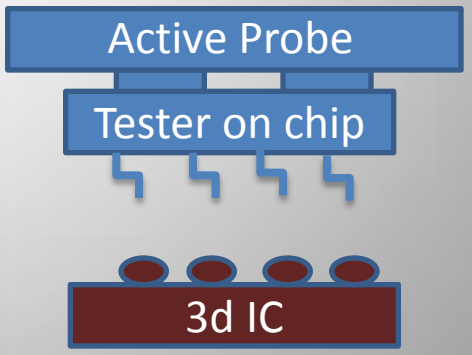
- Why test before stacking?
  - Design verification / Defect isolation
  - Reduces yield loss
  - Enables integration of chips from different suppliers

"Stack, Then Test",
Can be Achievable With
Available Technologies

"Test, Then Stack",
→ Need for Active Probe Card



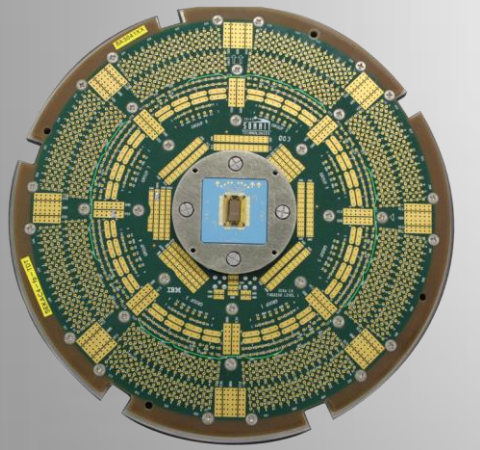




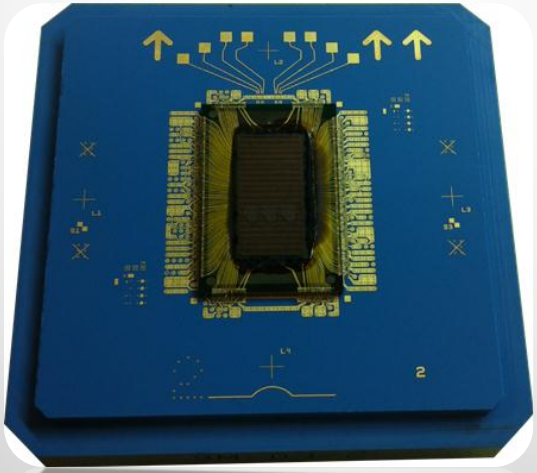
Active MEMS Probe Card

Silicon Valley Test Workshop

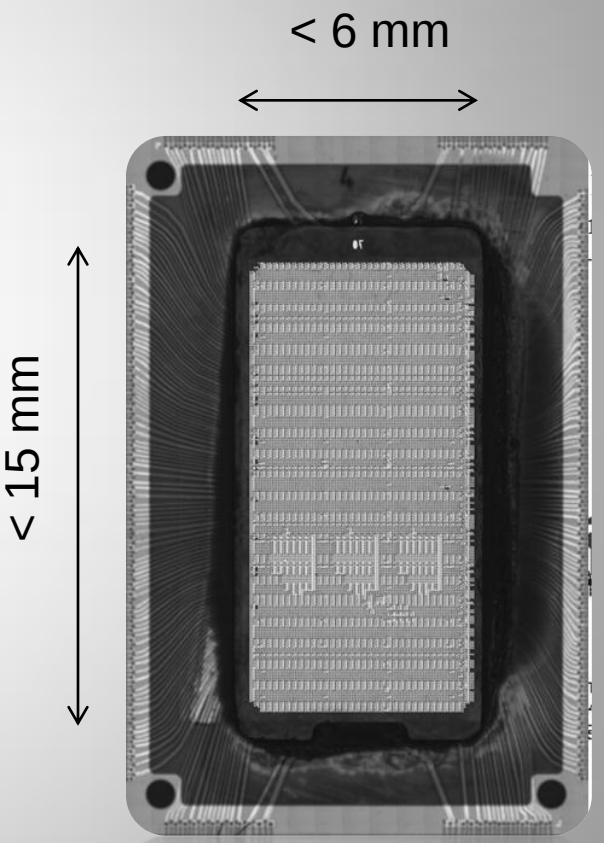
- Over 1300 IO's
- 50µm min pitch
- 5,000 Powers and Grounds
- Four (4) power planes



V93k platform

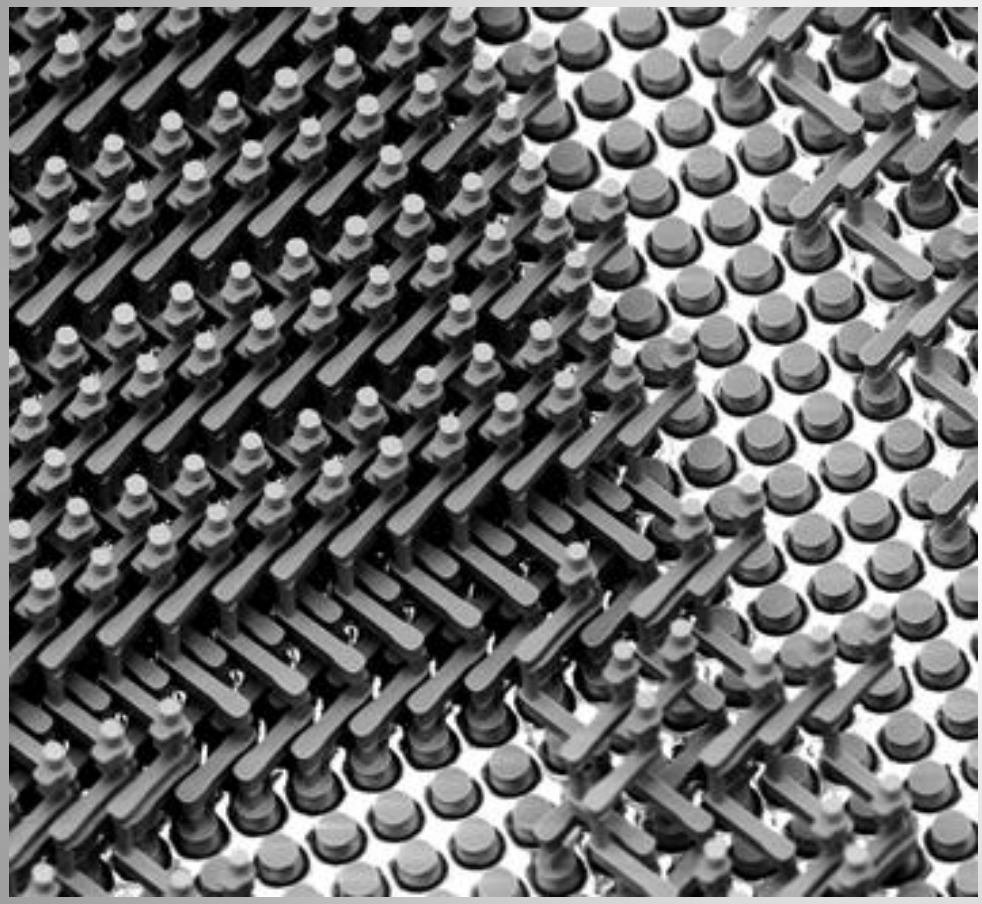


Probe head with Active die and MEMS Probes

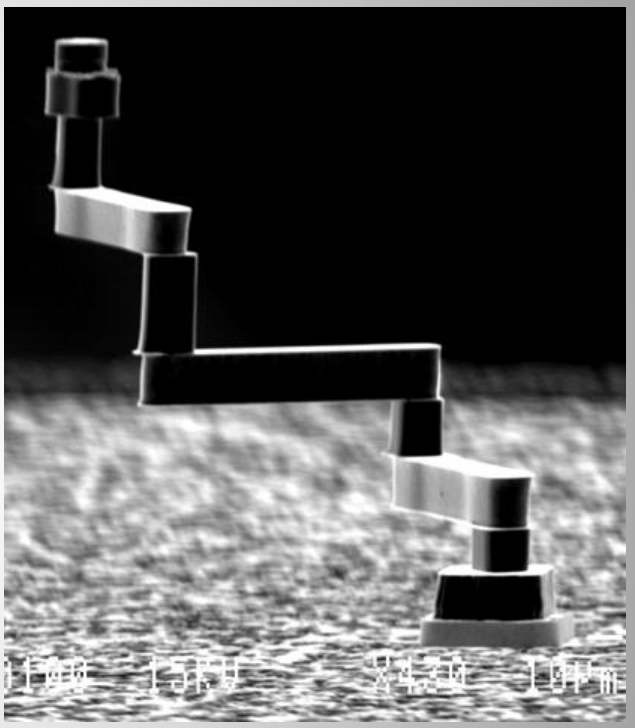


Top down view of the Active die and MEMS Probes

Active MEMS Probe Card



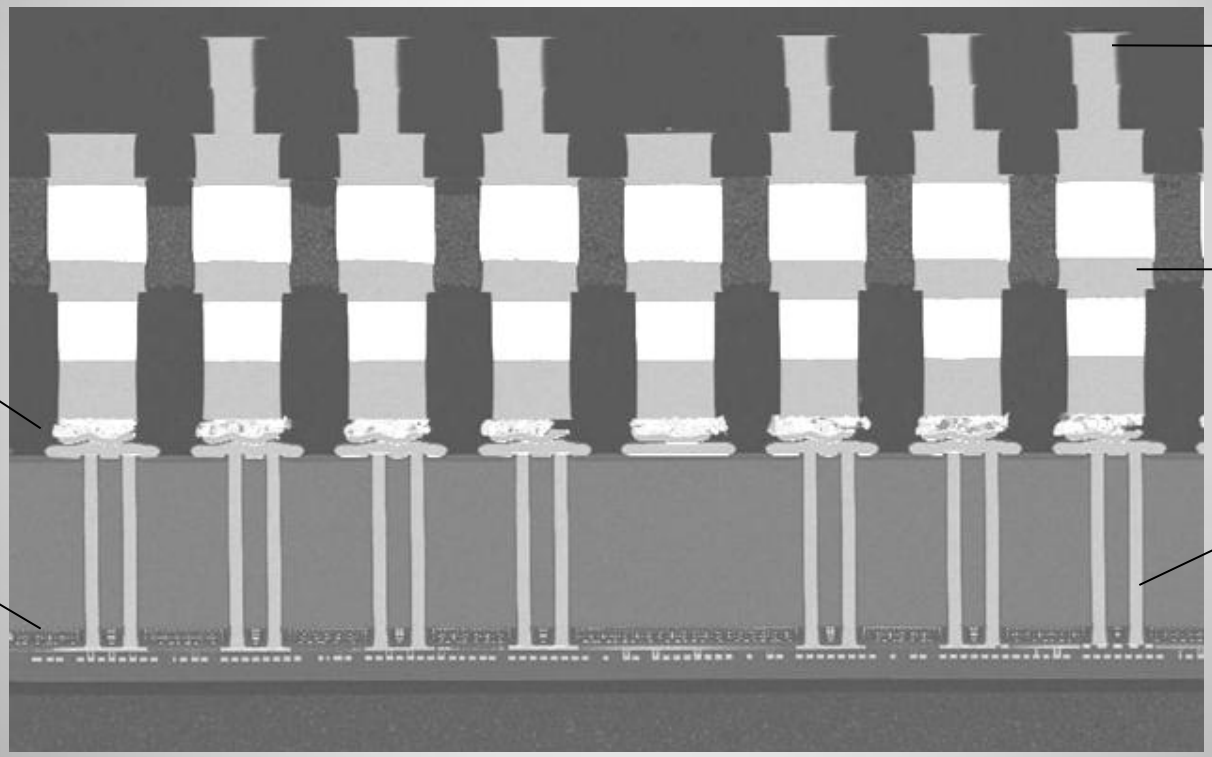
Detail of the Active PC, at 50um (minimum) pitch MEMS probes



Example of a Fine Pitch MEMS Probe

- Operating OD: 15µm
- Scrub Length: 10-15µm
- Force: 0.2 gF

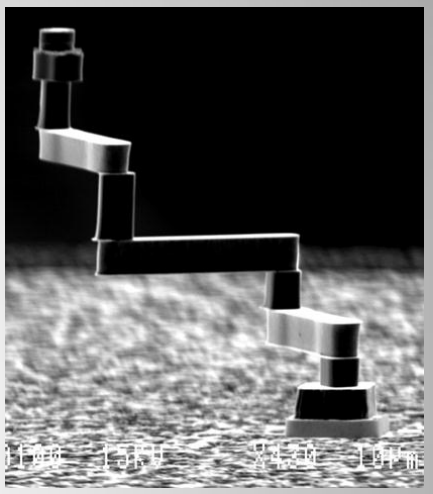
Active MEMS Probe Cross-Section



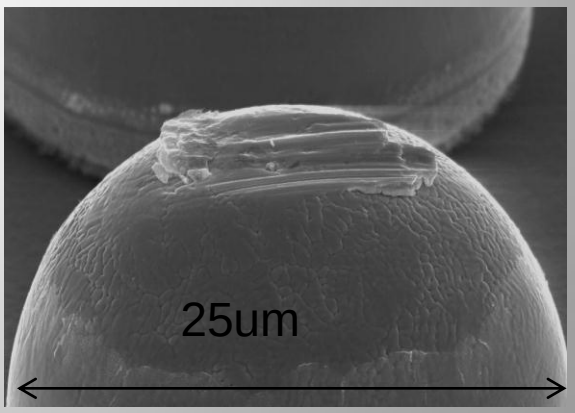
SEM: typical cross section of an Active die with MEMS probes

Low Force MEMS Probe

- Why MEMS?
  - Wafer Scale manufacturing
  - Lithographic scaling and planarization
  - No probe-count limitations
  - Short probe length for better electrical performance



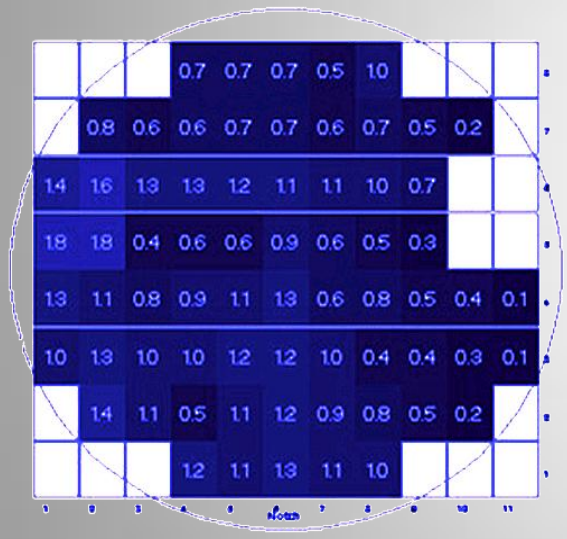
- Low Force?
  - Optimized high tip pressure (tip design) and scrubbing action (spring design) to achieve adequate CRES performance.
  - Minimal damage to all test contact surfaces
  - Enables inline product test



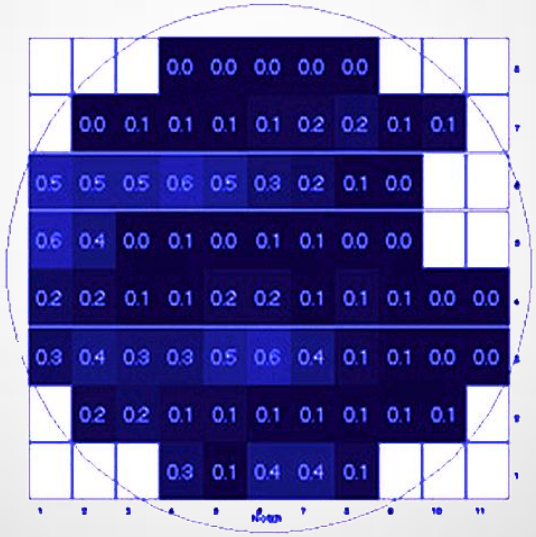
Example of a scrub mark on a 25um "uC4"

CRES on uC4

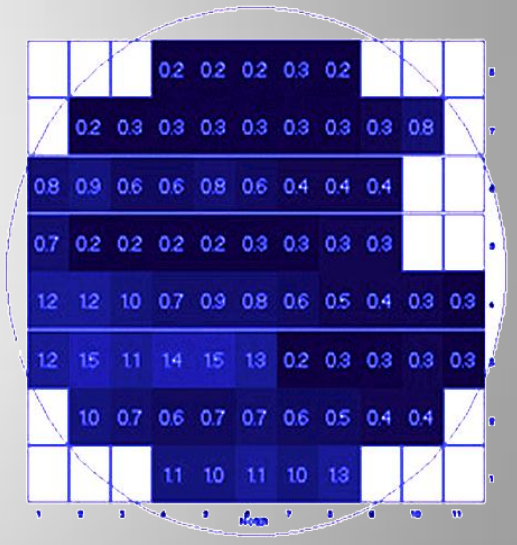
- Contact resistance on µC4 lead free solder bumps at -10C, 25C, and 85C
- Examples of Mean CRES* Value per Die, 52 channels, 100mA current:



14µm OD at -10C: <1.8Ω



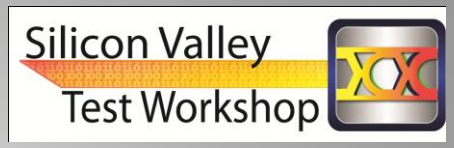
14µm OD at 25C: <0.6Ω



14µm OD at 85C: <1.5Ω

**CRES each channel = Resistance on bumps (Path + CRes) – Resistance on Gold (Path + CRes)*

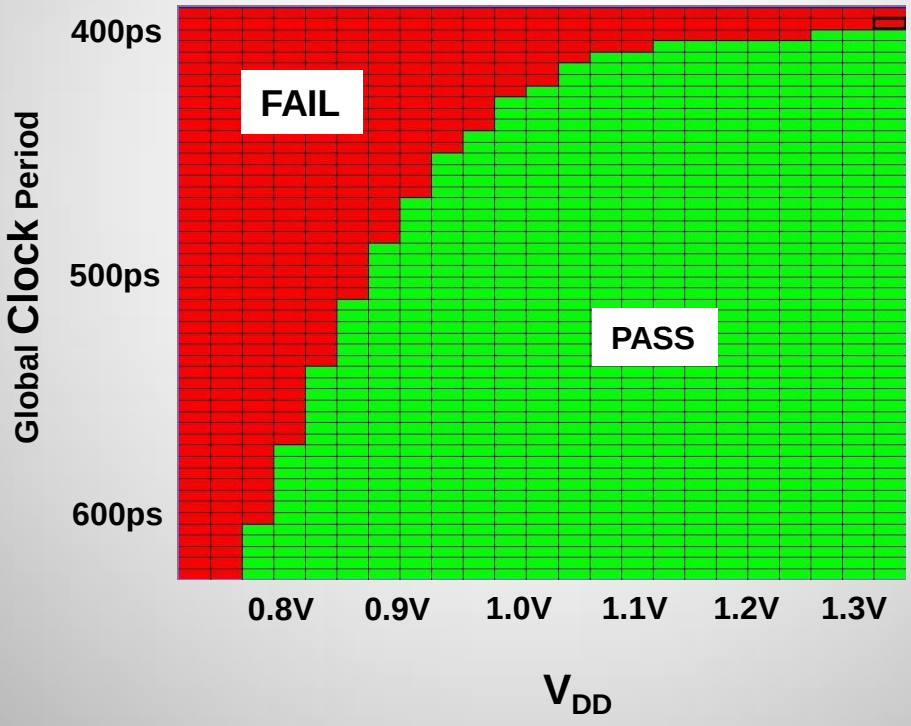
Functional Testing



- Wafer Test Flow
  - External IO and Inter-strata IO (ISIO) DC Pin Testing
  - Power Supply Shorts and Standby Current
  - Structural ATPG Scan and Logic Test
  - Array Built In Self Test (ABIST)
  - Performance Inter-strata Input / Output (ISIO) Test
- 3D Wafer Level eDRAM and ISIO AC Characterization
  - Fmax, Vmin / Vmax
  - Stack Power / Thermal
  - Logic , eDRAM, and ISIO Performance Measurements

eDRAM and ISIO Performance Test

- eDRAM, logic, etc. is 100 % tested through TSV, ISIO, C2C interconnects, Pre-stack for KGS



Fmax = 2.2 GHz , Vrange = .7v to 1.4v

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Dynamic Power and Thermal Monitoring

Silicon Valley Test Workshop

- Active Probe Card monitors die Thermal and Power Sensors dynamically
- Active MEMS Probe enables Very Fast Response Time
  for Power Switching, Voltage Regulation, and Clock Controls
- Flexible for Adaptive Test, Sequential Testing, and Chip Test Partitioning

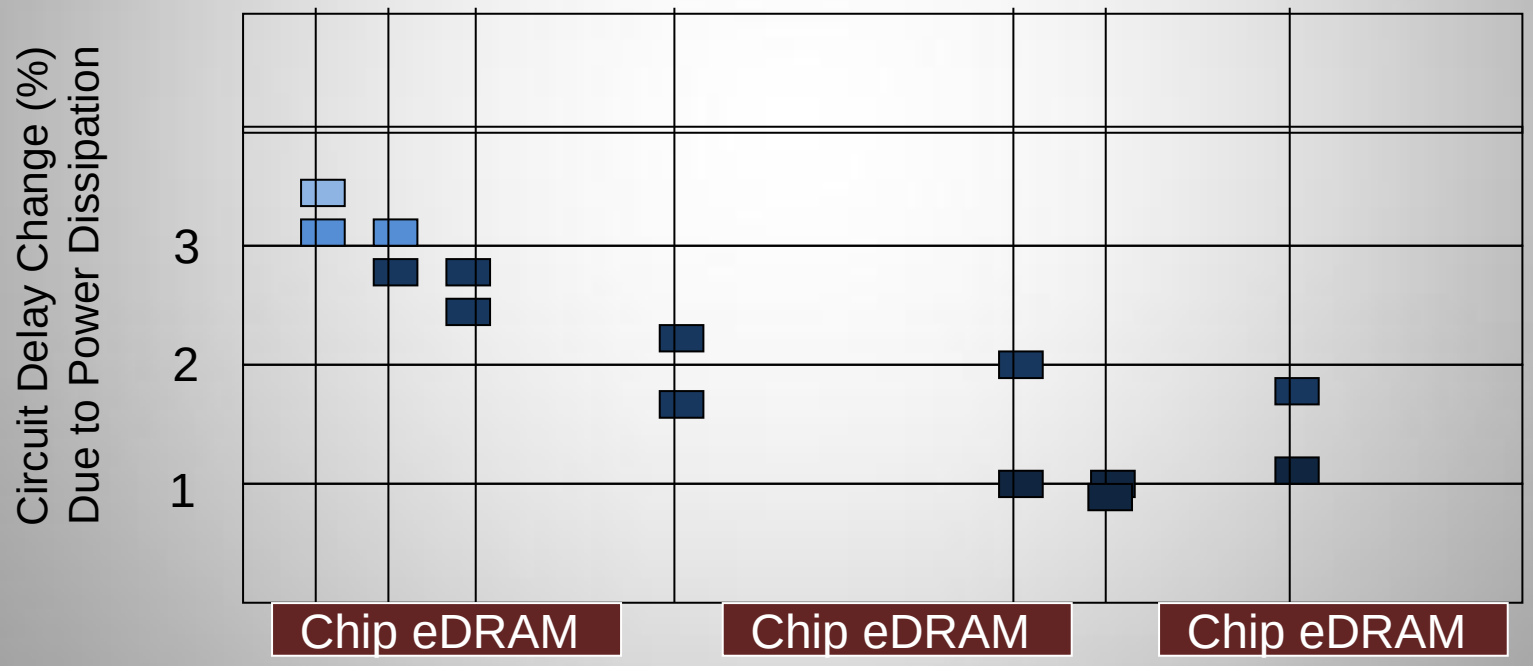
Instant Temperature Control by Active Probe Card reducing switching activity

Temperature Rise due to high switching activity

Example of a thermal "map" during testing

Performance Variation Localization

- Performance variation can be quickly measured and isolated with Active MEMS probe measurement systems for AC yield learning at wafer test



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Summary

- Bonded MEMS Probes to a thin Active Die with TSV, attached to a complex space transformer stack to form a fully functional probe card
- Demonstrated full DC and AC functional testing on 3D chips with 50µm pitch µPillars at the Wafer Level

Acknowledgements

- Gary Maier / IBM SRDC project lead, test development
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- Ting Hu / AAI Sr. Design Engineer
- Feng Lo / Lithography Manager
- Michael Chang / R&D Engineer
- Shahram Mehdizadeh / Sr. Plating Engineer
- Jane Tran / Packaging Engineer
- AAI Manufacturing & Quality Teams
- Greg Medrick / AAI General Manager , Advanced Probe Cards