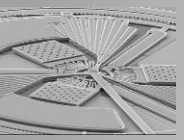
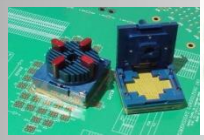
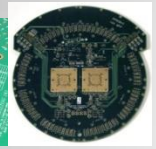
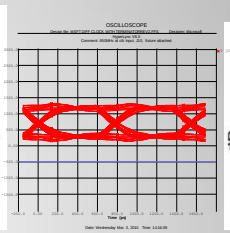
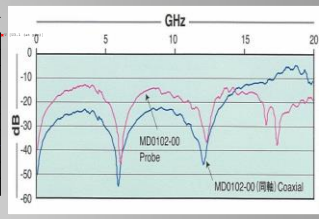
Silicon Valley Test Workshop

CYPRESS PERFORM



Testing a Programmable SOC

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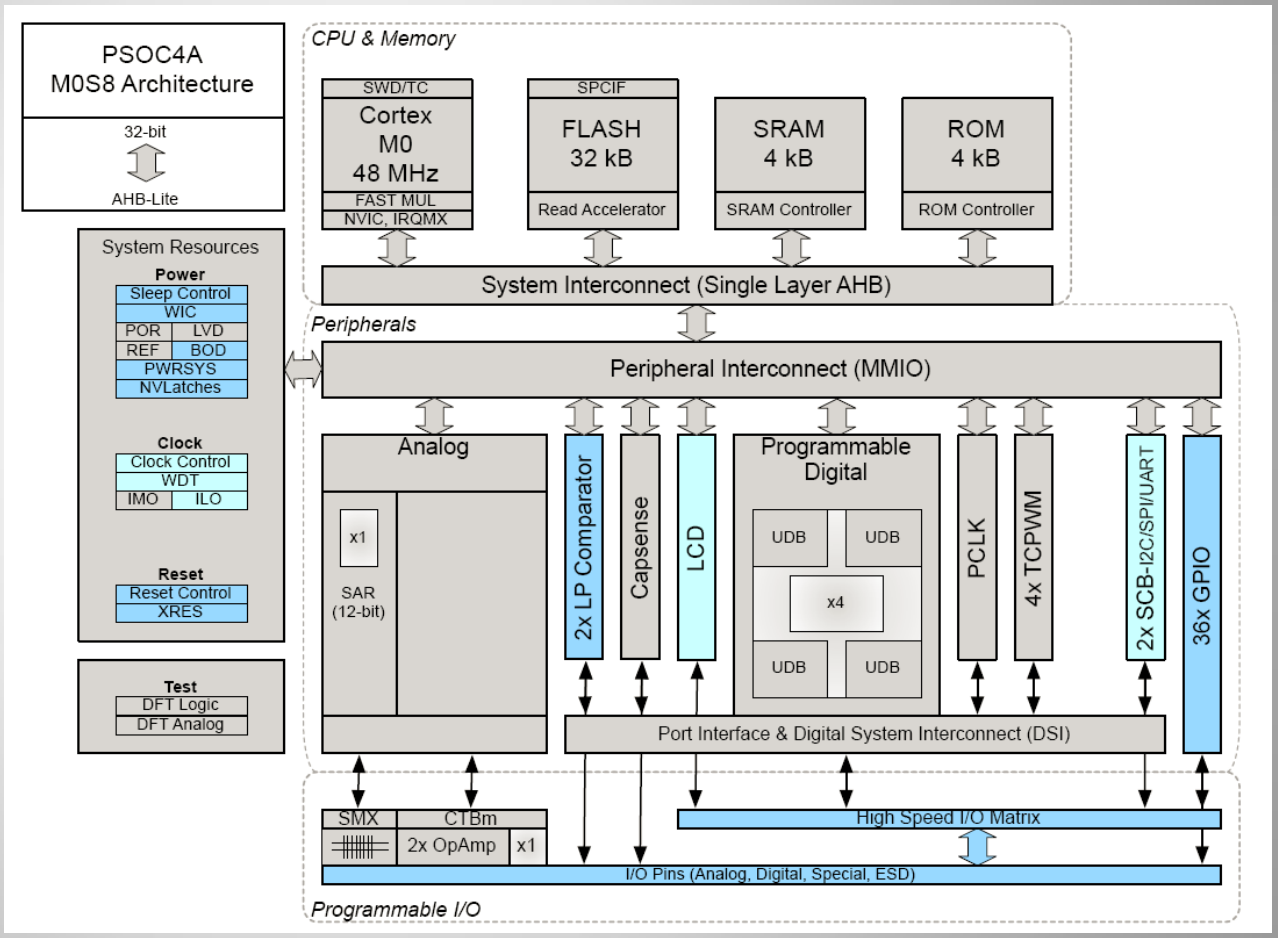
Outline

- Device Overview
- Device Applications
- Design For Test
- Test Challenges
- Silicon Shuttles
- Device Validation
- Characterization
- Production Test
- New Feature To Come

Device Overview

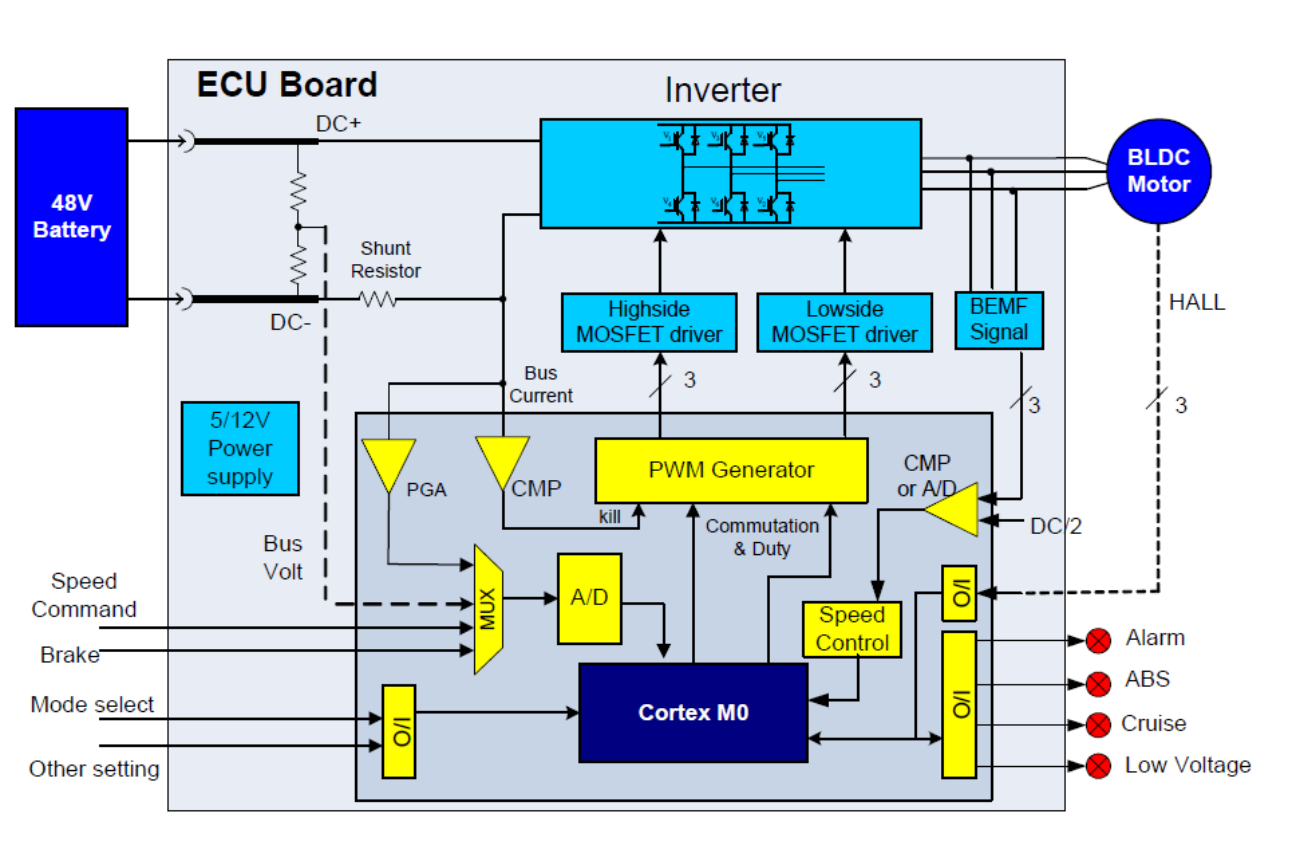
- Cortex M0
- 32k Flash
- 4k SRAM
- 36 GPIO
- PWMs
- Cap sense
- Comparators
- Opamps
- DACs
- ADC
- Development SW



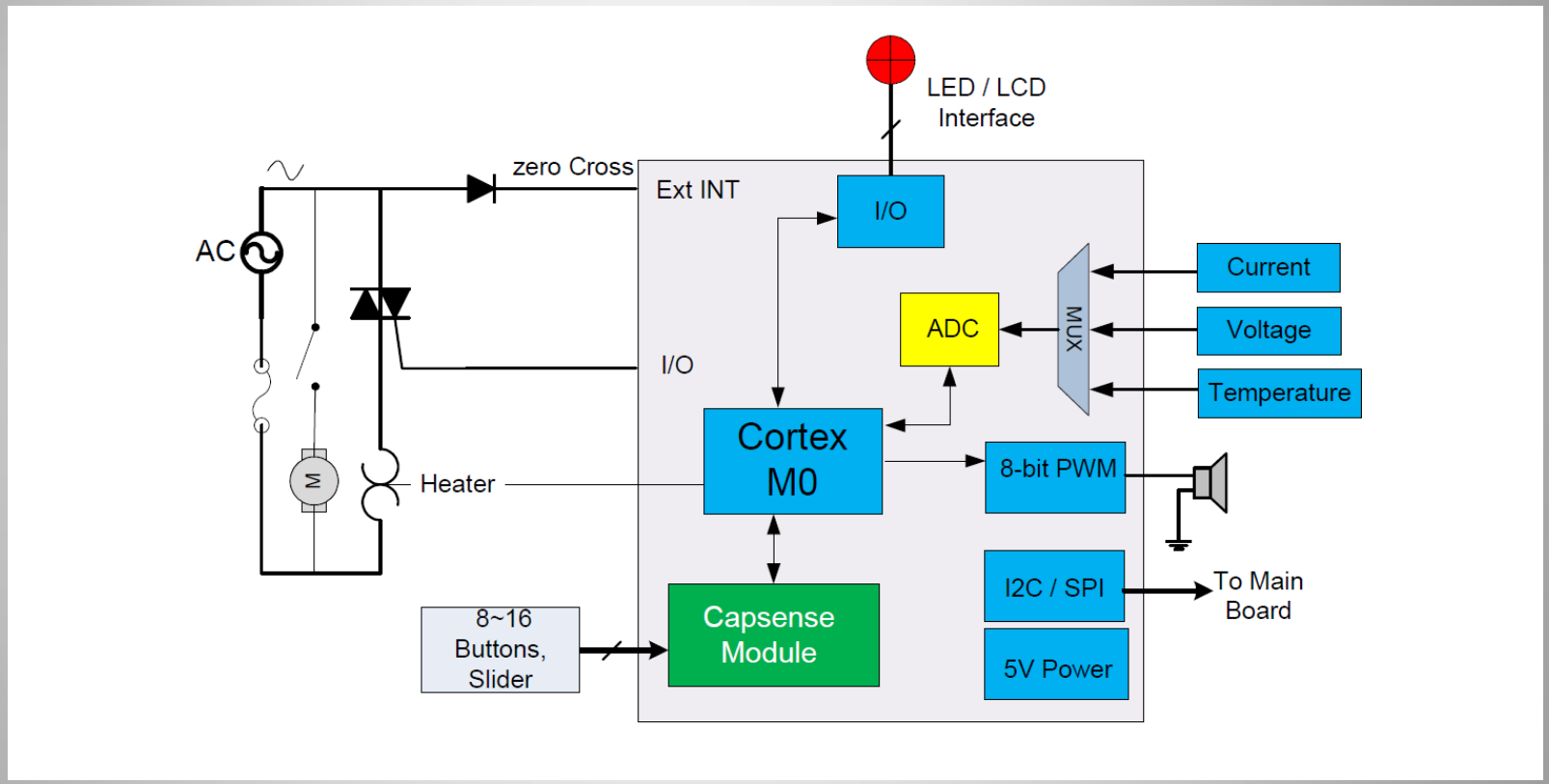
Device Applications

- Motor control
- Cap sense
- Water meters
- White goods panels
- Fish finders
- Induction cooker

Motor Control



Home Appliance Application



Test Challenges

- Many user interfaces
- Very low sleep current (< 20nA)
- Many parameters to test
- Most analog blocks need trim
- Flash test time is long

User Interfaces

- Fixed function
  - I2C
  - SPI
  - UART
  - LIN
  - Smart card reader
- Programmable through UDB
  - I2S
  - PRS
  - CRC
- Test
  - SWD, Serial wire debug
  - PTM, parallel test mode

Power Modes

- Active – 20mA
  - All resources active & clocked
- Sleep – 850uA
  - CPU inactive & not clocked
- Deep sleep – 0.5uA
  - CPU, SRAM, high speed peripherals off
- Hibernate – 150nA
  - All clocks stopped
- Stop – 20nA
  - All blocks off, GPIO retains state

Operation Modes

- Boot
  - Load trims
- Test
  - Scan
  - IP block access
- Debug
  - User program debug
- User
  - User developed code executes

Design For Test

- Serial & Parallel test interfaces
- Scan
- DDFT bus
- ADFT bus
- Flash test modes
- SRAM BIST
- Functional test
- Trim adjustments

Device Security

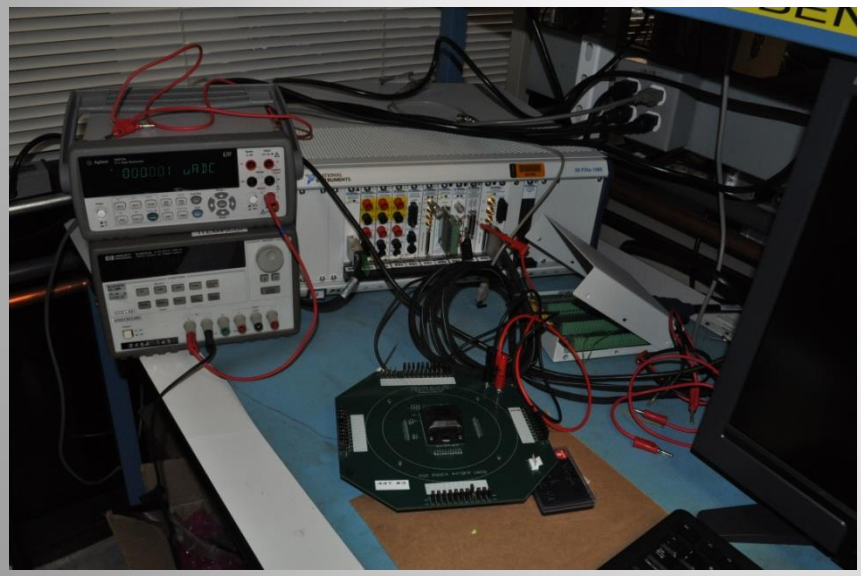
- Virgin
  - As delivered from fab, no trim
- Open
  - Trimmed, ready to program
- Protected
  - Ready to use, no access to user code
- Kill
  - No debug or test access available, irreversible

Silicon Shuttles

- Multiple IP blocks
- IP Fully accessible
- Cost allocated to product lines
- Quarterly tape outs
- Quick turn assembly

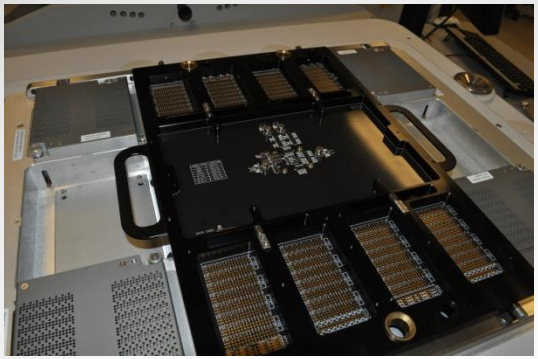
Device Validation

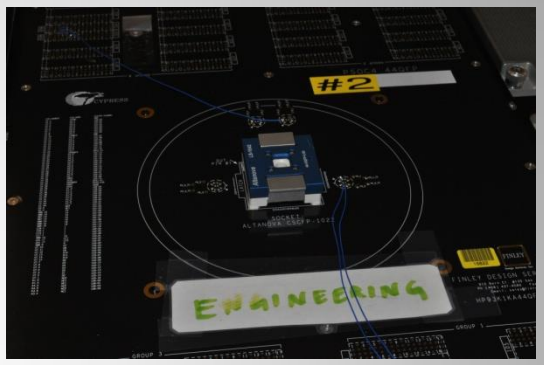
- Initial bring up
- Validate all blocks are functional
- Validate logic
- Check compliance to standards

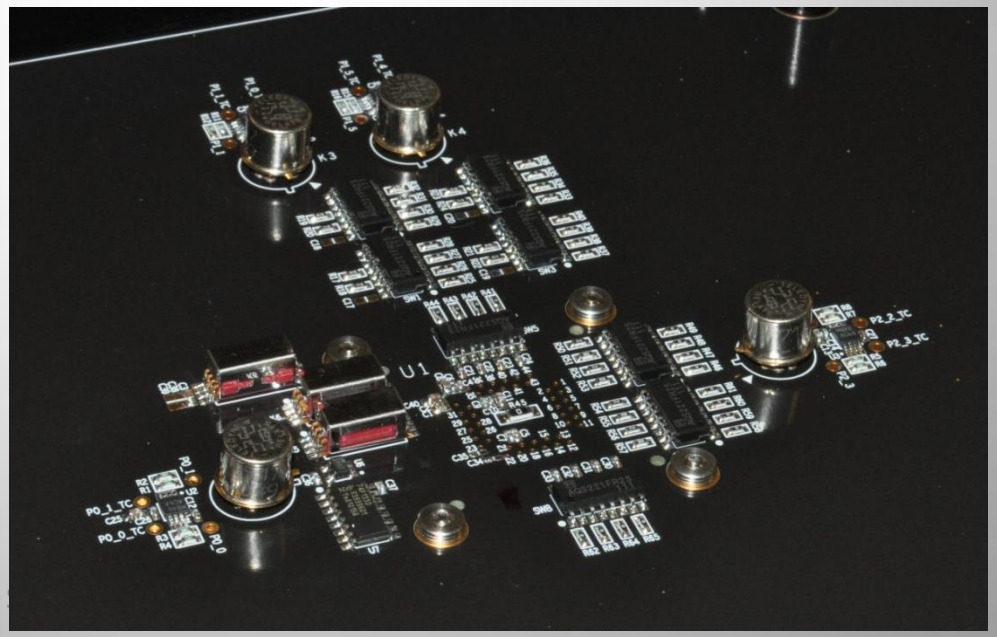


Characterization

- Digital timing
- IO voltages
- Supply currents in all power modes
- Static – INL/DNL/Gain/Offset/CMMR/PSSR
- Dynamic – THD/SNR







Production Test

- CTAS, Class Test At Sort
  - Test all parameters
  - Reduced pin count test allowed
- CTAC, Cheap Test At Class
  - Test for assembly defects, missing bond, die crack
  - Retrim parameters affected by packaging
  - Test all IOs

Test cost

- CTAS, Class Test At Sort
  - Parallelism as high as possible
  - Use reduced pin count to increase parallelism
  - Use only enough ATE
  - Don’t test parametrics with high Cpk in characterization
- CTAC, Cheap Test At Class
  - Parallelism limited due to handler
  - Don’t test parameters not affected by packaging
  - Shut off tests which never fail

Nextest Wafer Sort

Wafer Sort

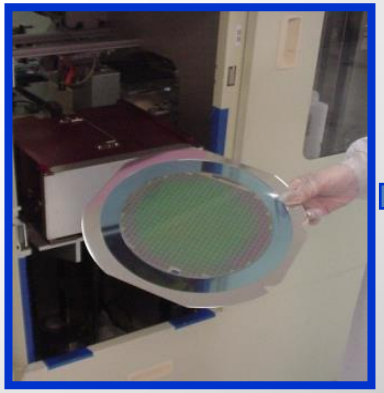
- Scan, covers PnR and CPU
- Flash/RAM/ROM
- Programmable digital blocks
- Analog trim
- DC parameters
- Routing – switch resistance
- Analog performance

Autoline Assembly & Test

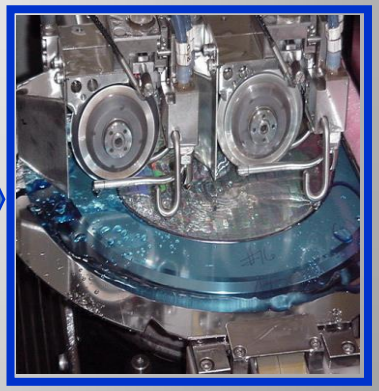
Die Prep Process

DIE BANK

BACKGRIND

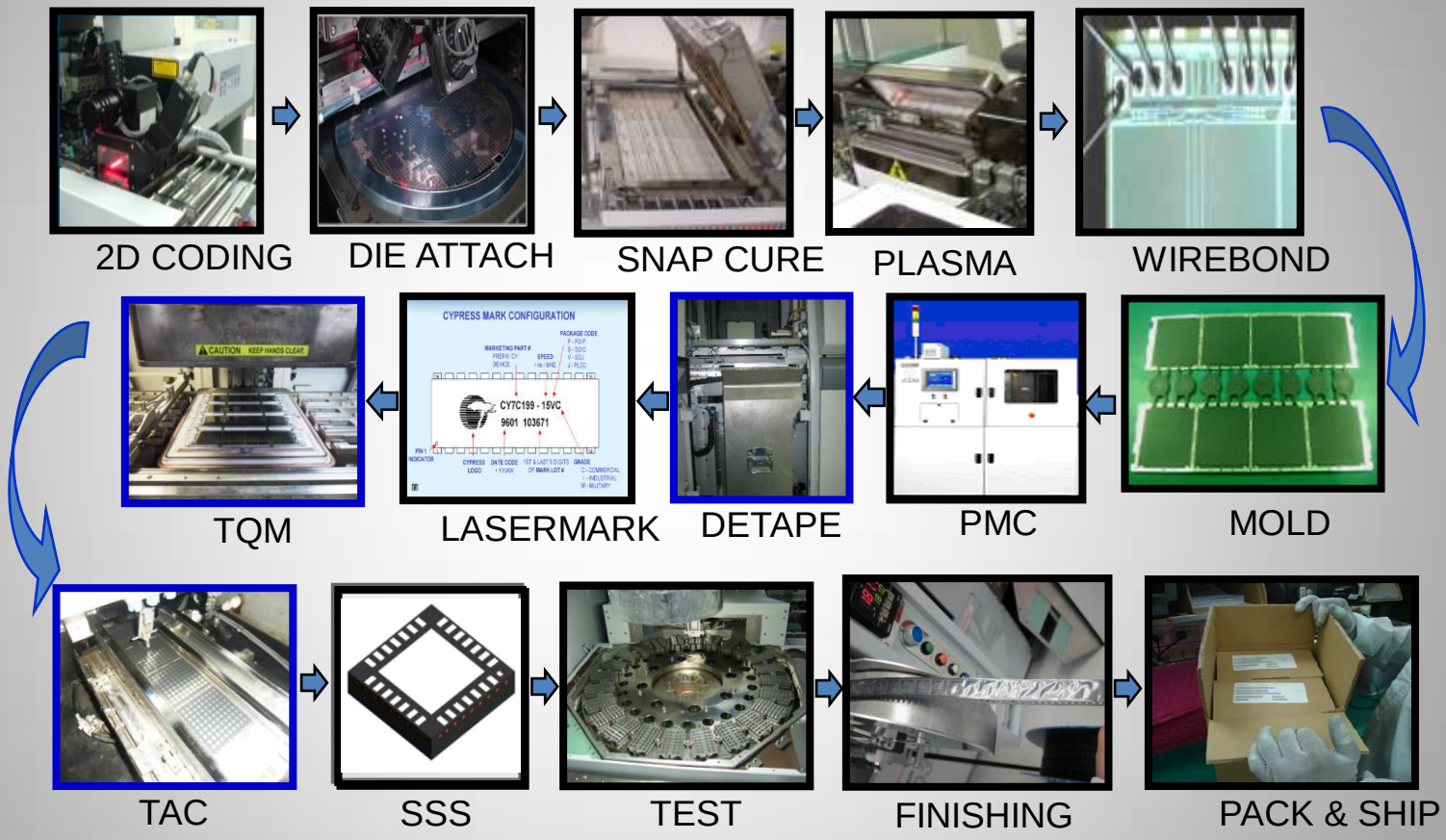


WAFER MOUNT



WAFER SAW

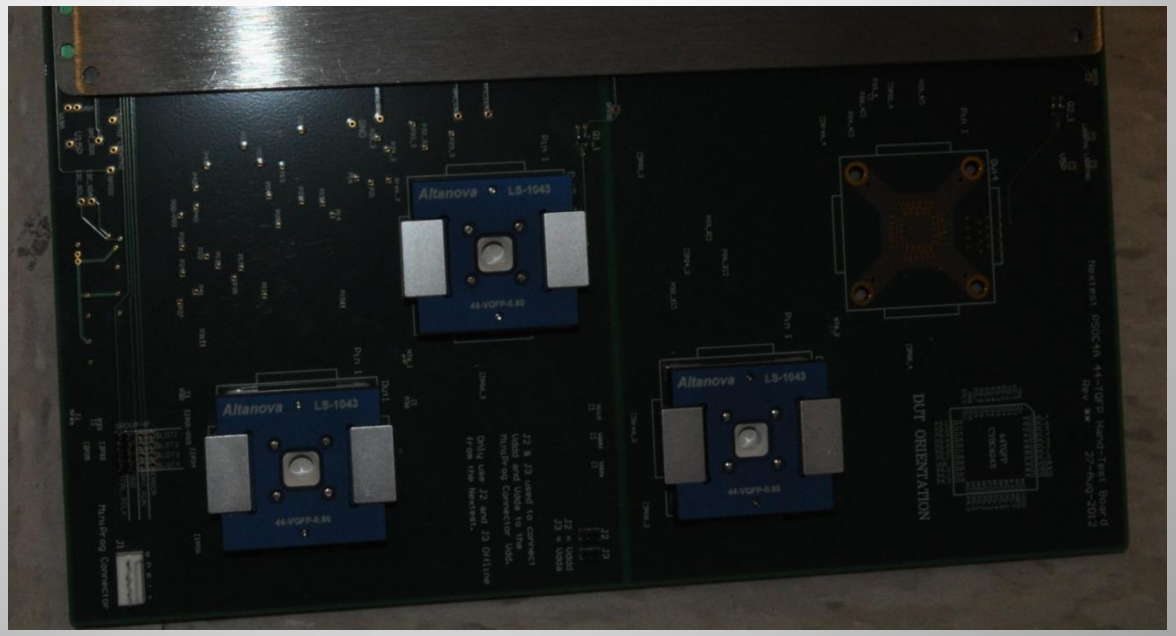
QFN Process Flow



Package Test

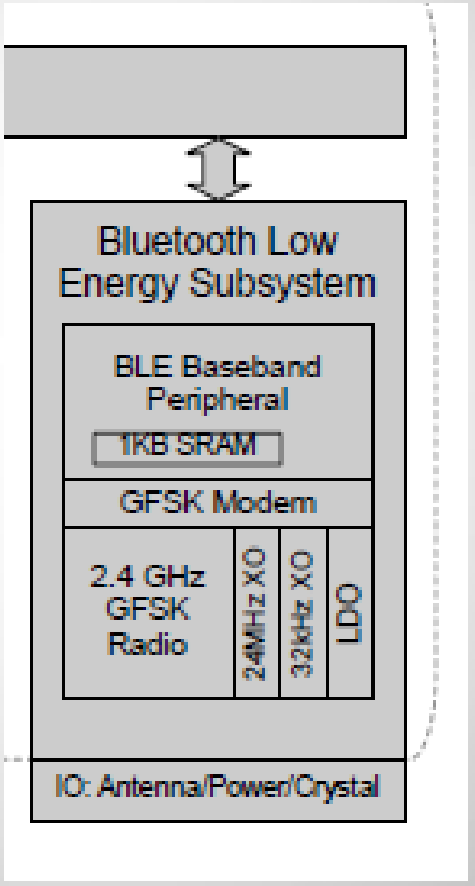
Package Test

- All IOs
- Scan, to check for die cracks
- Retrim parameters affected by package



New Features To Come

- More analog
- BTLE
- High frequency PLLs



Conclusions

- Design product for many applications
- Design to be ATE friendly
- Test for quality
- Control costs