

VRT:

The Test Escape You Cannot Escape From?

True or False

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Presentation Path

What is VRT

- Define the Behavior
- Root cause

Practical Implications

- Implications for manufacturing
- Implications for systems
- Paradigm change for test?

Conclusion



What is VRT?

Variable Retention Time (VRT) is the behavior of a storage cell that exhibits more than one data retention value.

It was first noted in a paper presented at the 1987 IEDM conference.

“A Meta-Stable Leakage Phenomenon In DRAM Charge Storage - Variable Hold Time”

(Yaney et al, AT&T Bell Laboratories)

“A new leakage phenomenon called Variable Hold Time(VHT) is reported which can compromise the data retention performance of modern DRAMs. Careful observations of retention(Hold) time on many devices with planar cells and grounded field plates has uncovered a very small portion of the bit population which exhibits multi-valued and metastable leakage current at room temperature. “

Mysterious VRT

1992 Paper presented at IEDM:

DRAM Variable Retention Time
(Restle et al.;IBM)

Paper reported on study that looked at DRAMs from multiple manufacturer's with multiple technologies(trench capacitor and stacked capacitor cells).

VRT was found on all chips!!!

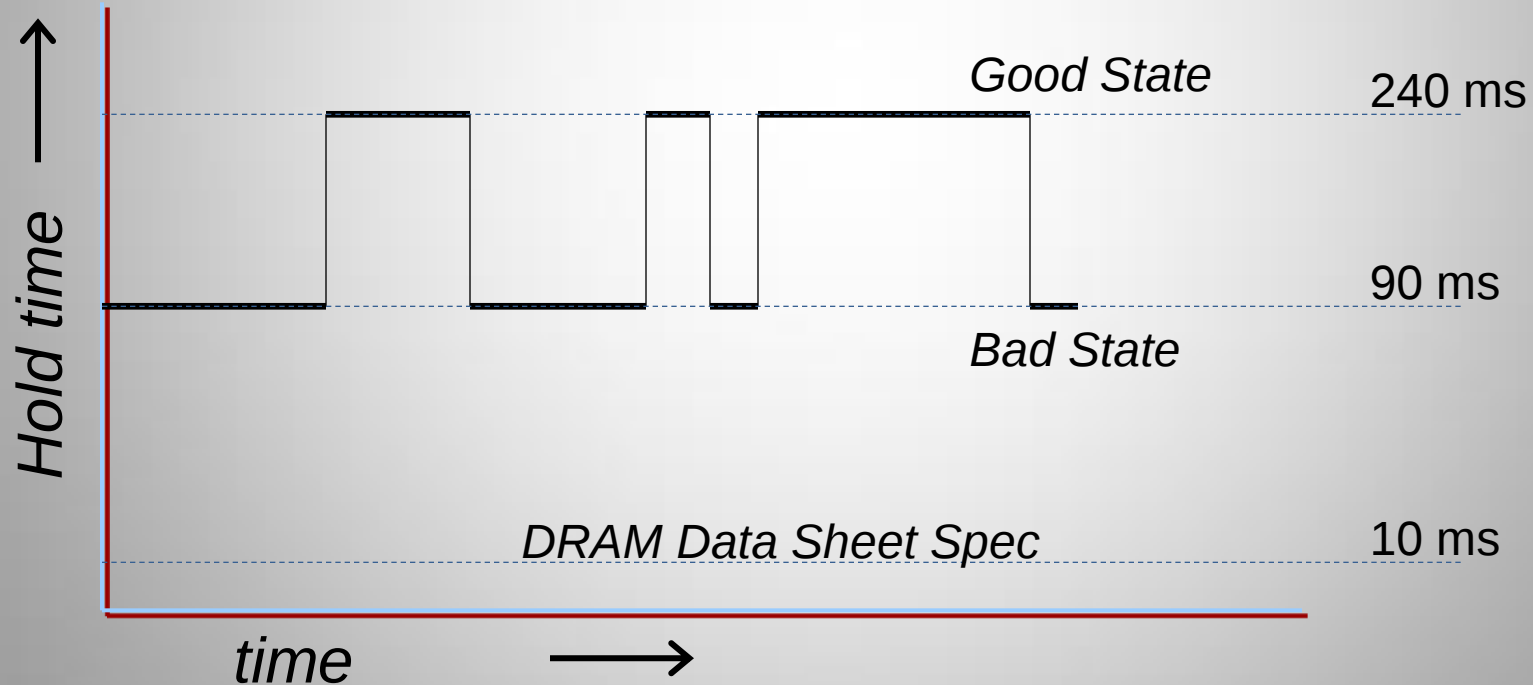


Both papers indicate the locations of VRT are associated with observed silicon anomalies but some cells in these areas exhibited VRT and some didn't.

VRT- So What?



After 1992 there were no significant papers presented on the subject until 2004.

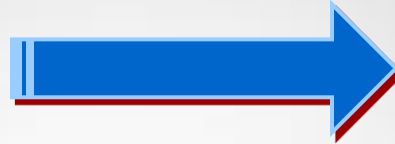




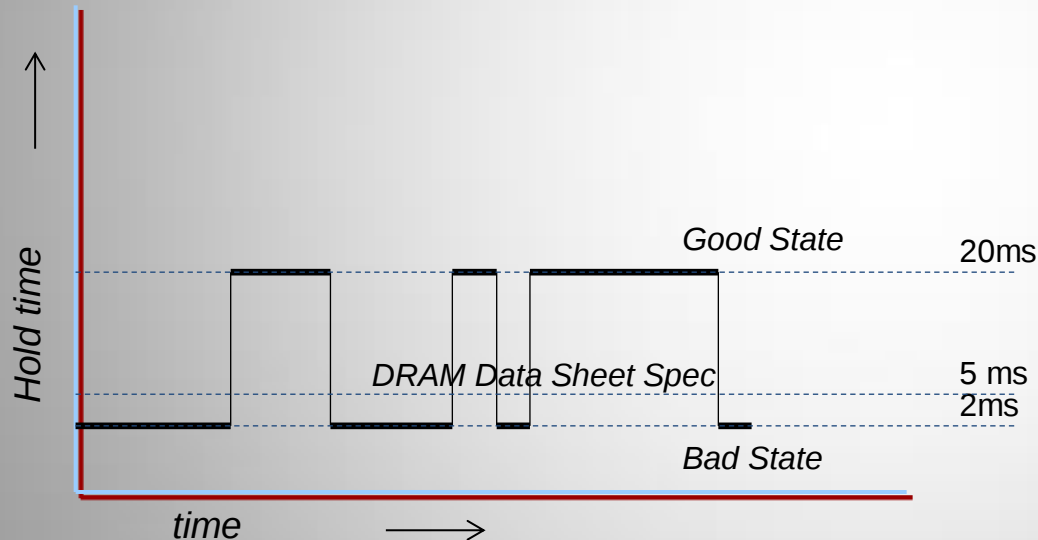
VRT: Changing Environment

Trends since 1992

- Smaller Geometries
- Smaller Chip Voltages



Smaller Cell Storage
Capacitance



Smaller Hold Times

VRT has become one of the most important issues in
dynamic random access memory (DRAM)

No Headroom



VRT is a Test Escape

There are two reasons why VRT represents a test escape.

1. VRT transitions between a Good and Bad Hold time are random.
2. A Good or Bad hold time state can stay stable randomly for milliseconds or hours.

2006: Single vacancy-oxygen complex defect and variable retention time phenomenon in silicon LSI (Umeda et al; Elpida/NEC)

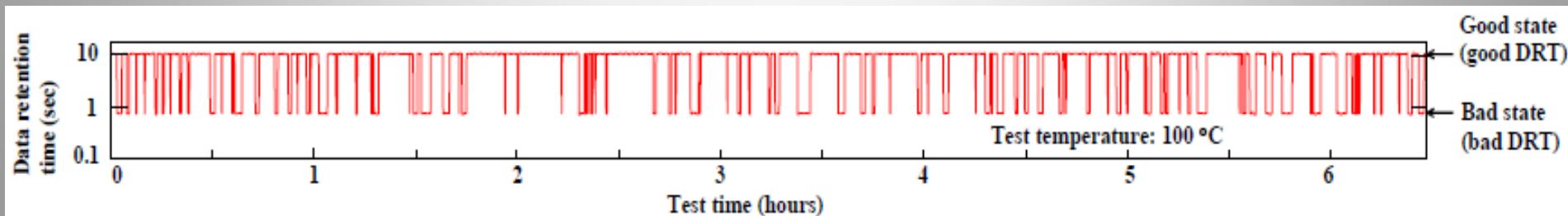


Fig. 1 Two-state variable retention time (VRT) in a DRAM bit.

VRT is a Test Escape

Random failures can be screened for given a long enough test time

- Increased test time adds cost to a product.
- Even with increased test time random appearance of the behavior means you never know for sure if you have screened the defect.



VRT: Abatement Strategies

VRT has been strongly linked to silicon defects.

Research and investigations have moved from recognizing the behavior to understanding the defect that causes VRT.



There are several silicon manufacturing strategies proposed to reduce VRT in memory chips

- Increase the retention time of the storage cell to add the margins back
- Decrease defects. Keeping in mind there are some process steps that by nature induce defects (i.e. ion implantation and dry etching)
- Make the passivation of the defect more thermally stable

VRT: System Design Considerations

Initial 1987 seminal paper concluded with the following statement

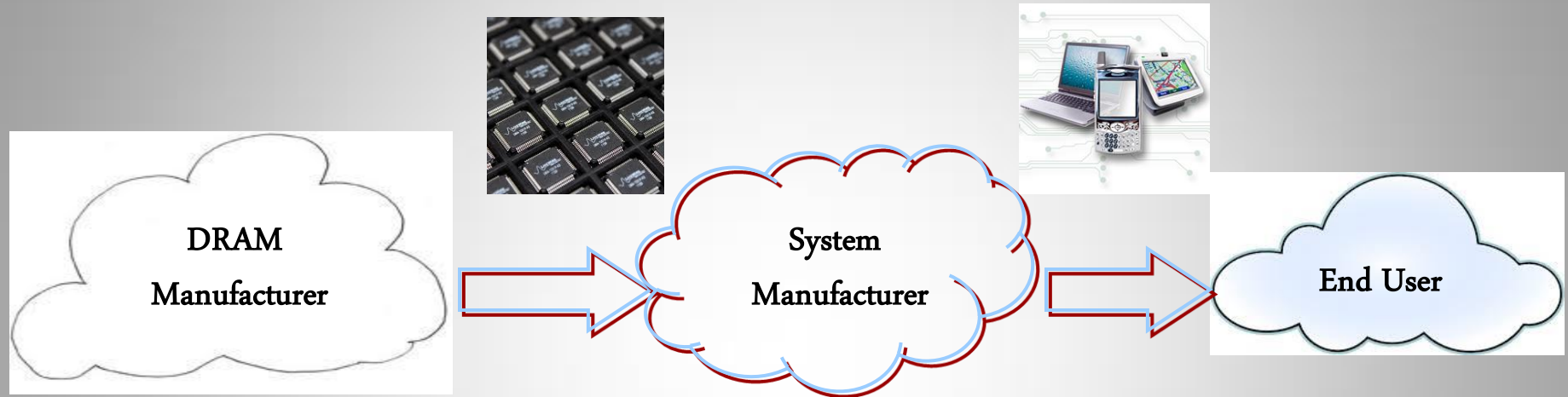
“VHT is random, bad bits may remain hidden during any screening test. These parts can then escape into the "good" population only to later exhibit what very much appears to be a soft error in the system application. We therefore recommend that no application of DRAM be made without error correction in some form.”

That is to say systems can be designed with enough error correction mechanisms to keep functioning even with memory devices that intermittently fail due to VRT failures as well as other soft error failure mechanisms.

There is a cost(both in \$\$\$ and performance) in adding error correction capabilities. The more error correction capability needed the higher the cost.



Device Life Cycle Test Strategy Typical for Today



- Chip Level ATE Testing
- Redundancy Repair (Stuck-At and Hold Time)

- Bed of Nails System Test
- BIST and System Diags

- *BIST and Diags*

- VRT Abatement Strategy
- No Direct Testing for VRT other than Hold Time Test

- Error Correction Mechanisms
- BIST and System Diags may opportunistically detect VRT failure

- Potential system failure if quantity of errors overwhelms Error Correction Mechanisms

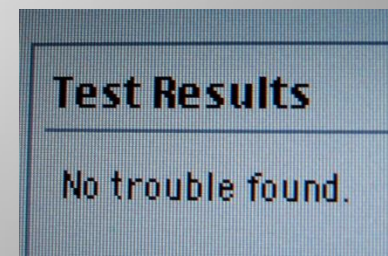
VRT Field Costs

It is very difficult to determine the field costs of VRT because of the elusive nature of the VRT behavior. Today's test methodology is not well developed and is designed to measure hold times and not designed to detect Variable Retention Time.

Without VRT Aware Test methodologies it can be very difficult to detect a memory failure due to VRT.

- VRT fails act like a soft error because they may fail intermittently
- VRT fails appear like a hard fail in that the failure reoccurs at the same address(es) or if the transition period is large enough.

How many NTF Failure Analysis results have been due to VRT behavior???



VRT Field Costs

In the 2009 paper

“DRAM Errors in the Wild: A Large-Scale Field Study”

Schroeder(Univ of Toronto), Pinheiro(Google), Wolfe(Google)

They noted

“we observe DRAM error rates that are orders of magnitude higher than previously reported, with 25,000 to 70,000 errors per billion device hours per Mbit and more than 8% of DIMMs affected by errors per year.

“About a third of machines and over 8% of DIMMs in our fleet saw at least one correctable error per year.”

“The annual incidence of uncorrectable errors was 1.3% per machine and 0.22% per DIMM.”

“If an error is uncorrectable, i.e. the number of affected bits exceed the limit of what the ECC can correct, typically a machine shutdown is forced. In many production environments, including ours, a single uncorrectable error is considered serious enough to replace the dual in-line memory module (DIMM) that caused it.”

Hold Time Test

Hold Time (cell or region)

1. Write a One to the cell(s)
2. Wait for a time interval(Data sheet refresh spec t_{REF})
3. Read the cell(s)

If a cell contains a Zero and the time interval is less than t_{REF} than the cell is considered a failure and must be repaired or ignored





VRT Test: Methodology Requirements

A VRT Test is looking for variation in hold time.

- It follows that a VRT Test requires a cell(s) hold time to be measured at least two times. The more frequently the measurement is performed the better the chance of detecting a variance.
- A VRT Test therefore requires the ability to store hold time measurements for individual cells.

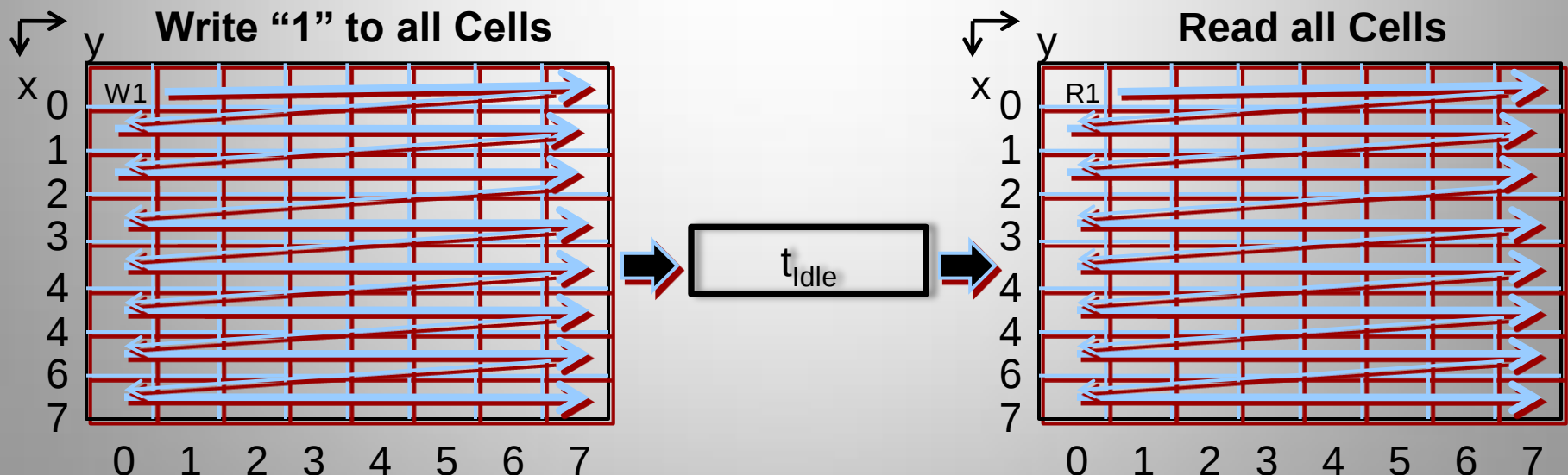


VRT Test: Efficient Execution



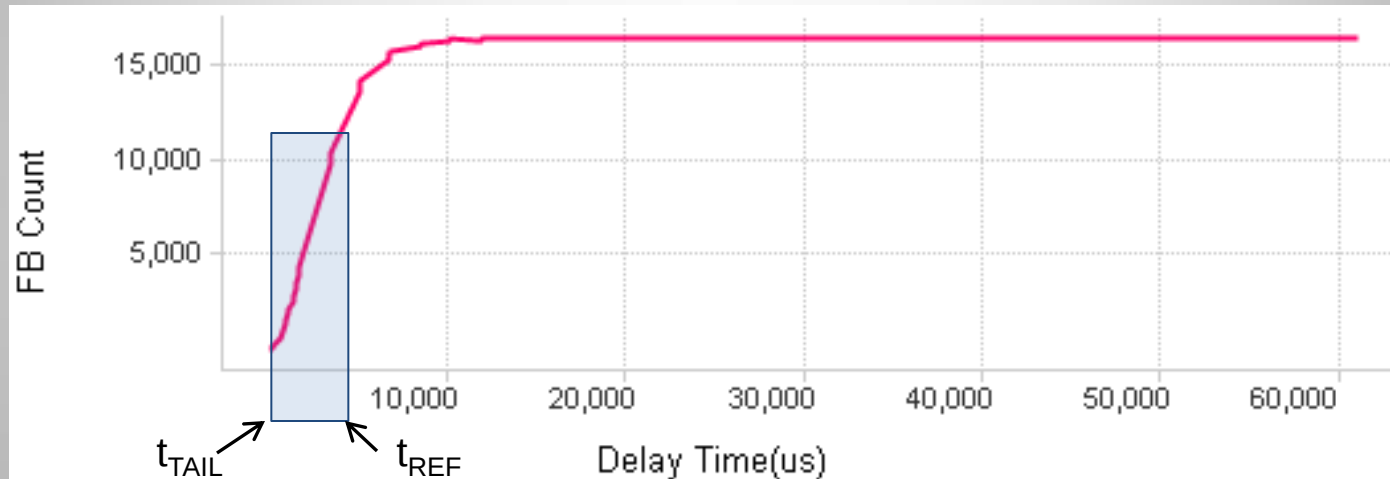
- Hold Time Tests are expensive tests because the wait time(t_{Wait}) needed to check for data decay is typically measured in milliseconds. Measure as many cells as possible to use the time as efficiently as possible. Minimize t_{Idle} by Writing and Reading as many cells as possible at the device's maximum clock rate(t_{CLK})

$$t_{\text{Wait}} = ((x_{\text{bits}} * y_{\text{bits}}) * t_{\text{CLK}}) + t_{\text{Idle}}$$



VRT Test: Focused Analysis

- Hold time measurement wait times (Delay Times) only need to cover the region between the cell with the shortest hold time (t_{TAIL}) and t_{REF}



- For each region of cells t_{TAIL} must be determined by using a search method. Using a linear search with a multiplied step followed by a binary back search provides fast tail detection

Improved VRT Aware Test Method



- Run hold time measurement tests as fast as possible
- Tests as many bits as possible simultaneously
- Store results of all Hold Time Measurements
- Choose appropriate search parameters
- Test only the bits needed to be tested



Improved Device Life Cycle

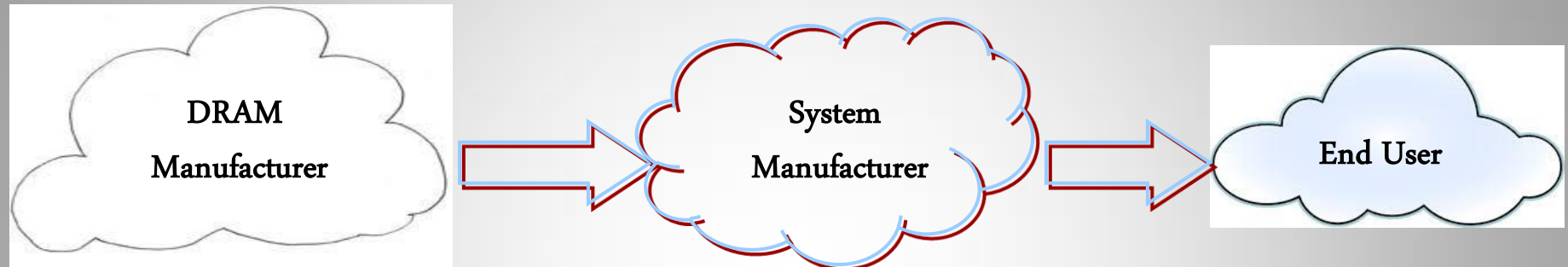
VRT Test Methodology

- Develop Test Methods that are capable of detecting VRT(VRT Aware).
Use VRT Aware Test Methods in device manufacturing tests and include VRT Aware Test Methods in System BIST to provide detection and resolution over the device life cycle.
- Since the occurrence of VRT is random
Statistical Models are required to determine how much test time is needed to achieve the desired level(s) of VRT-free quality. Statistical Models are developed from characterization data supplied by a VRT Aware Test Method
- Design system with appropriate amount of Error Correction and Memory repair capability over the device life cycle



Device Life Cycle Test Strategy

VRT Aware



Extend the VRT Testing over the device life cycle

- Chip Level ATE Testing
- Redundancy Repair (Stuck-At, Hold Time and VRT)

- VRT Abatement Strategy
- If all VRT cells cannot be repaired device may still be usable in VRT aware systems

- Bed of Nails System Test
- BIST and System Diags

- Error Correction Mechanisms
- BIST and System Diags include VRT Test capability to detect VRT cells during system manufacture and in field
- Further Redundancy Repair can be used to fix detected VRT cells or they could be set to be ignored by error correction logic

- *BIST and Diags*

Paradigm Change for Test



In last year's presentation I asked the following questions without providing answers. This year I can provide answers:



How do you deal with a “Test Escape You Cannot Escape From”?

Is it acceptable to ship devices that have suspected but undiscovered defects? (Yes)

Is there value in a test solution that finds SOME defects? (Yes)

If you detect a VRT cell and repair it how do you know the repair is free from VRT defects? (Improve VRT Testing Methodologies use VRT Aware Device Life Cycle Test methodology)

Characterization is Critical

Characterization of VRT behavior in Gbit DRAMs is an expensive endeavor because the hold time test must be performed many times for each memory cell to monitor the hold time variance.

Since the VRT transitions occur randomly in time extensive hold time Characterization Data **combined** with Statistical Analysis is critical to:

- Development of a test strategy designed to provide varying levels of VRT free quality
- Continued monitoring of the Test Strategy in DRAM manufacturing
- Development of Error Correction Mechanisms in system design which provide a capability that is appropriate to VRT free quality of the DRAMs in the BOM



Conclusion

VRT is becoming a new problem for the industry

- It's behavior makes it elusive to 100% detection.
- It is pervasive in all devices that have storage cells that use a pn junction.
- Ten years ago VRT could be considered an interesting behavior today it has become a costly if not a fatal behavior.
- A VRT Aware Test methodology is possible which will detect cells that exhibit VRT behavior
- A VRT tolerant system is possible through appropriate use of Error Correction Mechanisms and the implementation of VRT Aware BIST and system diagnostics